"PULSED MEASUREMENTS ON HETEROJUNCTION DEVICES"

**Final Technical Report**

by

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United States Army

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# SUMMARY

This report summarizes the results obtained by the University of Padova (Consorzio Padova Ricerche) and the University of Roma, Tor Vergata, in the framework of the project "Pulsed measurements of heterojunction devices", funded by the European Research Office of the U.S. Army (contract N68171-98-M-5803). The objective of this project has been the understanding of the physical limitation of GaAs and InP microwave devices by means of DC and pulsed measurements, and of Monte Carlo 2D device simulations.
Breakdown of GaAs-based MESFETs and HEMTs, and of InP-based HEMTs has been studied by means of a Transmission Line Pulse (TLP) technique in the 20 - 500 ns range. Results can be summarized as follows: (a) due to the non negligible influence of thermal effects on breakdown characteristics, and to the presence of unstable portions of I-V curves of the devices, TLP is the only technique which enables a realistic evaluation of on-state breakdown characteristics of power devices; (b) by measuring non-destructively the on-state breakdown curves up to gate current density levels never reached in the literature, we show that breakdown is triggered by a self-regenerative effect due to a parasitic bipolar action and is quenched by high injection and thermal effects occurring at high drain currents; (c) this analysis of on-state breakdown mechanisms is confirmed by Monte Carlo simulations. On the basis of the experimental observations, an equivalent circuit model of breakdown suitable for circuit SPICE-like simulations has been developed.
The impact ionization coefficient of holes in $In_{0.53}Ga_{0.47}As$ has been measured by means of pnp Heterojunction Bipolar Transistors. Our data are in good agreement with independent results obtained by means of photoavalanche measurements.
The described experimental procedures and theoretical analyses provide viable tools for the evaluation and modeling of on-state breakdown and burn-out effects in power microwave devices.

**LIST of Keywords:** Microwave devices;
High Electron Mobility transistors (HEMT's);
Heterojunction Bipolar Transistors (HBT's);
Pulsed measurements;
Breakdown;
Reliability

# INTRODUCTION

A better understanding of device physics, together with improved technologies, has lead to the development of high power, high voltage microwave devices. Recent reports have shown that GaAs-based C-band pseudomorphic HEMTS can be fabricated within standard processes with breakdown voltages in excess of 30 V at $I_D/W$ = 400 mA/mm [1], while InAlAs/InGaAs HEMTs adopting a $p^+$-InGaAs/p-InAlAs/InP gate layer and regrown $n^+$-InGaAs ohmic contacts achieved an off-state breakdown voltage of 31 V, on-state breakdown 7 V, with $I_D/W$ = 300 mA/mm [2]. InGaP/GaAs double heterojunction bipolar transistors with $f_{max}$ = 115 GHz and breakdown voltages $BV_{CE0}$ = 27 V have been fabricated [3]. If the requirements on operating frequency are relaxed, breakdown voltages as high as 70 V can be achieved.

These results, and the current development of GaN- and SiC- active devices, with extremely high operating voltages, emphasize the need of techniques capable of characterizing hot carrier effects such as impact ionization, and the consequences on advanced devices, such as breakdown, burn-out and reliability issues.

A previous report (under contract N68171-97-C-9034) has studied hot-electron effects, breakdown and reliability in FETs, HEMTs, and HBT's" by means of DC characterization techniques. This report summarizes the results obtained by the University of Padova (Consorzio Padova Ricerche) and the University of Roma, Tor Vergata, in the framework of the project "Pulsed measurements of heterojunction devices", funded by the European Research Office of the U.S. Army (contract N68171-98-M-5803). The objective of this project has been the understanding of the physical limitation of GaAs and InP microwave devices by means of pulsed measurements in the ns time scale, and of Monte Carlo 2D device simulations.

Results can be summarized as follows:

(i) The impact ionization coefficient of holes in $In_{0.53}Ga_{0.47}As$ has been measured by means of single Heterojunction Bipolar Transistors. In order to correctly evaluate sources of errors, a suitable model has been developed; results have been corrected for Early effect and temperature increase due to self-heating. Data are in excellent agreement with results obtained from photomultiplication measurements and Monte Carlo simulations.

(ii) A Transmission Line Pulse system has been set up, which allows the non-destructive evaluation of breakdown characteristics of MESFET and HEMT devices. This method has several advantages with respect to the conventional ones: (a) it allows a non-destructive evaluation of on-state breakdown up to very high current densities; (b) device self-heating, which affects conventional measurements, is avoided; (c) unstable portions of the I-V output characteristics can be measured; (d) high voltages and currents can be obtained simply, by charging the transmission line with a suitable high voltage DC generator. For these reasons, this method should be useful also for the testing of GaN and SiC high breakdown voltage devices.

(iii) The on-state breakdown characteristics of several GaAs-based MESFET and HEMT devices have been experimentally characterized. In on-state, breakdown is identified by a remarkable increase in output conductance, $g_D$, determined by impact ionization; $g_D$ has the same non-monotonic behavior on $V_{GS}$, $I_D$ as the gate current due to impact ionization. At high $V_{DS}$, a positive feedback mechanism induces a very steep increase in drain current, which leads to device burn-out, unless high injection and thermal effects quench carrier multiplication. In off-state, regeneration induces a snap-back of the I-V characteristics.

(iv) Monte Carlo simulations of impact-ionization effects in GaAs-based pseudomorphic HEMTs explain the feedback mechanism leading to on-state breakdown as due to the parasitic bipolar action of holes, accumulated in the gate-source region of channel and substrate. The presence of the holes leads to increased injection of electrons in the channel, and therefore, to increased impact ionization.

(v) On the basis of the experimental results, and of Monte Carlo device simulations, a compact model, suitable for circuit simulations, has been developed, which reproduces correctly both pre-breakdown effects (slight increase in $|I_G|$ and output conductance) and full breakdown conditions (snap-back, gate current density above 1 mA/mm, catastrophic increase in output conductance)

Specific results are summarized at the end of each Section.

To the aim of comparing the results obtained during the last year under the contract N68171-98-M-5803 with those of the previous report (contract N68171-97-C-9034), this report is organized using the same structure of the previous one.

The first Section describes measurements and modeling of the hole impact-ionization coefficient of InGaAs lattice-matched on InP, obtained by means of suitable HBT devices. The second Section is devoted to the analysis of on-state breakdown in pseudomorphic HEMTs by means of pulsed measurements, and Monte Carlo simulations. Finally, an equivalent SPICE circuit model of MESFETs/HEMTs including impact ionization effects is described. Conclusions follow.

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E. Zanoni, G. Meneghesso and R. Menozzi "Electroluminescence and other Diagnostic Techniques for the Study of Hot Electron Effects in Compound Semiconductor Devices" (INVITED PAPER) Abstract of DRIP-VIII, The 8th International Conference on Defects-Recognition, Imaging and Physics in Semiconductors, p.XII-5, Narita, Japan, September 15-18, 1999.

E. Zanoni, G.Meneghesso, D. Buttari, M. Maretto, G. Massari, "Hot Electrons and Reliability in HEMTs" (INVITED PAPER) Proc. of WOCSDICE '99, 23th European Workshop on Compound Semiconductor Devices and Integrated Circuits, pp.39-42, Chantilly, France, May 26-28, 1999.

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Proc. of ESSDERC '99, 29th European Solid State Device Research Conference, pp. 548-551 Stuttgart, Leuven, Belgium 13-15 September 1999.

E. Zanoni, G. Meneghesso, A. Bortoletto, M. Maretto, G. Massari, D. Buttari "On-state breakdown measurements in GaAs MESFETs and InP-based HEMTs"
Proc. of 26th 120International Symposium on Compound Semiconductor, ISCS'99, Berlin, Germany, August 22-26, 1999.

G. Meneghesso, G. Massari, D. Buttari, A. Bortoletto, M. Maretto and E. Zanoni "DC and Pulsed measurements of on-state breakdown voltage"
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E. Zanoni, G. Meneghesso and R. Menozzi "Electroluminescence and other Diagnostic Techniques for the Study of Hot Electron Effects in Compound Semiconductor Devices"
To be published in the Journal of CRYSTAL GROWTH

E. Zanoni, G. Meneghesso, D. Buttari, M. Maretto, G. Massari, "Pulsed measurements and circuit modeling of a new breakdown mechanism of MESFETs and HEMTs"
To be presented at IRPS 2000, International Reliability Physics Symposium.

D. Buttari, A. Chini, G. Meneghesso, E. Zanoni, D. Sawdai, D. Pavlidis, S.S.H. Hsu, "Hole Impact Ionization Coefficient in (100)-Oriented $In_{0.53}Ga_{0.47}As$ based on pnp InAlAs/InGaAs HBTs"
Submitted to Indium Phosphide and Releted Material Conference 2000.

E. Zanoni, G. Meneghesso, A. Di Carlo, P. Lugli, L. Rossi, "Factors limiting the maximum operating voltage of microwave devices", Proc. of Advanced Workshop on Frontiers in Electronics (WOFE) 1999, pp. 103-104, to be published also in the Int. Journal of High Speed Microelectronics.

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# Chapter 1

# Fully Electrical Measurements of Hole Impact Ionization Coefficient in (100)-Oriented $In_{0.53}$ $Ga_{0.47}As$

## 1.1 Impact Ionization on $In_{0.53}$ $Ga_{0.47}$ As HBT's

*Abstract*— The hole multiplication factor in pnp $In_{0.52}$ $Al_{0.48}$ As/$In_{0.53}$ $Ga_{0.47}$ As single heterojunction bipolar transistors (HBT's) has been measured as a function of base-collector bias. Hole impact ionization coefficient $\alpha_p$ has been estimated taking into account the Early effect, $I_{CBO}$ and thermal effects. Numerical corrections for dead space and Kirk effects were made. Presented data agree well with previous photomultiplication measurements from Osaka et al., supporting them against those from Pearsall et al., the only one other source of data available in literature.

# 1.2 Device Technology

## 1.2.1 Layer Structure and Fabrication Process

The devices analyzed in this report are pnp $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ HBT's designed and grown at the *University of Michigan*, USA. Device technology is described in [1] and is reported here for convenience of the reader.

Device epilayers were grown [1] by solid-source molecular beam epitaxy on Fe-doped semi-insulating (001) InP.
The growth rate was 0.7μm/h at 490°C, and an $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ superlattice was grown on the substrate to improve the material quality. The layer structure is reported in Table 1.

| Layer | Type | Size (Å) | Doping ($cm^{-3}$) |
|---|---|---|---|
| Emitter cap | $p^+$ $In_{0.53}Ga_{0.47}As$ | 2000 | $2\times10^{19}$ |
| | $p^+$ $In_{0.52}Al_{0.48}As$ | 700 | $1\times10^{19}$ |
| Emitter | $p$ $In_{0.52}Al_{0.48}As$ | 1500 | $8\times10^{17}$ |
| Spacer | $i$ $In_{0.53}Ga_{0.47}As$ | 100 | — |
| Base | $n^+$ $In_{0.53}Ga_{0.47}As$ | 500 | $5\times10^{18}$ |
| Collector | $p^-$ $In_{0.53}Ga_{0.47}As$ | 3000 | $3\times10^{16}$ |
| Subcollector | $p^+$ $In_{0.53}Ga_{0.47}As$ | 5000 | $1\times10^{19}$ |
| Buffer | $In_{0.53}Ga_{0.47}As$ / $In_{0.52}Al_{0.48}As$ superlattice | ~ 1000 | — |
| Substrate | Semi – insulating (001) InP | | |

Table 1: $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ single HBT layer structure.

The reported background doping for undoped $In_{0.53}Ga_{0.47}As$ layers was below $5\times10^{15}\,cm^{-3}$, and undoped $In_{0.52}Al_{0.48}As$ layers were semi-insulating. Ti/Pt/Au and Pt/Ti/Pt/Au ohmic contacts were deposited on $n^+$ $In_{0.53}Ga_{0.47}As$ and $p^+$ $In_{0.53}Ga_{0.47}As$, respectively [1, 2]. The uniform $5\times10^{18}\,cm^{-3}$ base doping resulted in a sheet resistance of 76 Ω/□ and a contact resistivity to Ti/Pt/Au of $1.0\times10^{-6}\,\Omega\,cm^2$.

Devices were fabricated using a process derived from the high-performance npn HBT process described in [2] and reported here for convenience of the reader.

After deposition of the emitter ohmic contact (Pt/Ti/Pt/Au), the wafer was etched down to the base layer by repeated selective wet etches of the emitter cap, emitter, and spacer layers. The base metal, Ti/Pt/Au, was deposited self-aligned along two parallel edges of the emitter finger, such that the emitter undercut profile under the emitter metal was identical under all self-aligned edges. The emitter etching times were carefully designed to reliably obtain an emitter undercut so that the lateral distance

from the self-aligned base metal to the emitter semiconductor was 0.2 μm. In order to reduce extrinsic base-collector junction capacitances, the emitter fingers were protected with photoresist patterns while the base semiconductor layer was etched away self aligned to the base metal contacts. This step effectively reduced the semiconductor junction areas to those directly under the emitter and base metallizations. After the Pt/Ti/Pt/Au collector metallization was patterned and lifted off, the HBT's were isolated from one another to the semi-insulating InP level through a wet etch. The same wet etch was used to form trenches in the semiconductor under the emitter and base metallizations, which isolated the semiconductor in the intrinsic device areas from the semiconductor under the airbridge contact pads. The junctions under the airbridge pads are therefore isolated and do not contribute to parasitic capacitances ($C_{be}$ and $C_{bc}$). Finally, gold airbridges were electroplated to connect the HBT's to interconnects and coplanar pads. Nominal HBT emitter dimensions varied from 1-finger $1\times10\,\mu m^2$ to 10-finger $5\times40\,\mu m^2$, with typical values of $2\times10\,\mu m^2$ and $5\times10\,\mu m^2$ for high-frequency performance and high-power performance, respectively.

Measurements were performed on single-finger HBT's with an emitter geometry varying from $2\times10\,\mu m^2$ to $5\times40\,\mu m^2$.

# 1.3 Device operation

## 1.3.1 Punch-Through Collector

The non-negligible value in collector doping ($N_A$=3×10$^{16}$ cm$^{-3}$) results in a non-uniform electric field inside the collector region. Assuming a built-in voltage of about 0.7V, full depletion is reached at a base-collector voltage of about 1.1V. In Fig. 1 electric field distributions at various base-collector voltages are shown.

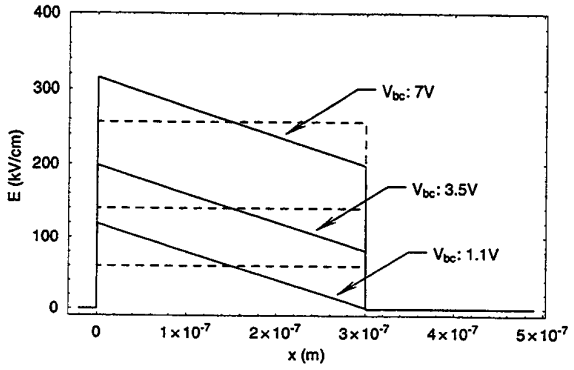


Fig. 1: Electric field distribution at the varying of the base-collector voltage ——— actual field - - - - average field

# 1.4 Device Characterization

## 1.4.1 Quasi-Saturation Effects, Recombination Currents and Parasitic Resistances

The forward I-V curve for a $2\times30\,\mu m^2$ HBT (JP2C) is shown in Fig. 2. The reported breakdown voltage $BV_{ECO}$ (at 10 A/cm$^2$) for a $5\times10\ \mu m^2$ sample [1] was 5.6V, and the offset voltage is 0.20V, in accordance with [1].

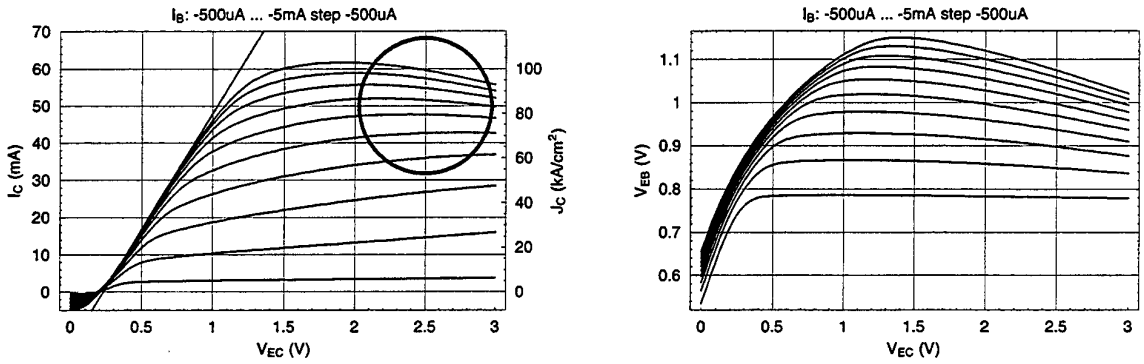


Fig. 2: HBT JP2C Emitter area: $2\times30\mu m^2$ $I_{Csafe}$: 30mA $I_{Cmax}$: 120mA

From the Gummel plot (Fig. 3), the ideality factors $n_B$ and $n_C$ are 1.85 and 1.00, respectively. These data are consistent among different devices, as shown in Fig. 4.

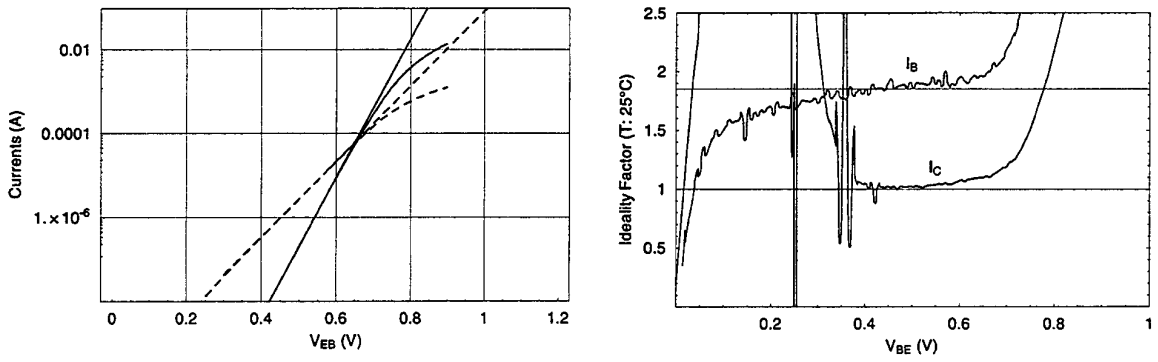


Fig. 3: HBT JP2C Emitter area: $2\times30\mu m^2$ $I_{Csafe}$: 30mA $I_{Cmax}$: 120mA
Left: ——— collector current – – – base current

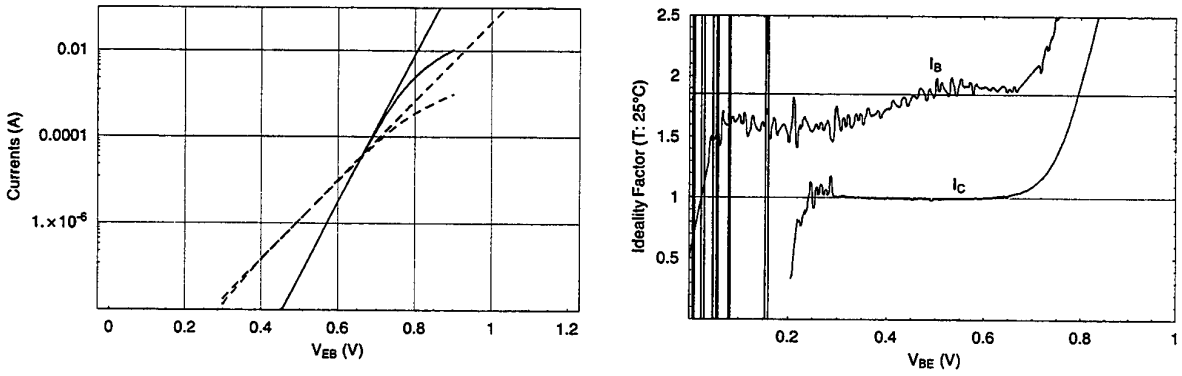


Fig. 4: HBT JP3A Emitter area: 5×10μm² $I_{C_{safe}}$: 25mA $I_{C_{max}}$: 100mA
Left: ——— collector current – – – base current

Previously reported ideality factors for a single-finger 5×10 μm² HBT were 1.60 and 1.00 [1]. The base current can be descrived by the following equation, with an ideality factor $\eta \simeq 2.0$,

$$I_B = I_{S_B} \exp\left(\frac{q V_{EB}}{\eta kT}\right) \tag{1}$$

which rules out neutral base recombination, and suggests the presence of dominant recombination processes. These processes could take place in the base-emitter space charge layer or at the base surfaces. Base-emitter electron injection is ruled out due to the high conduction-band offset voltage between $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ (0.48 eV [4]).

The dominance of recombination current affects only the base-emitter current and does not affect the collector current, which consist almost entirely of collected holes that are injected at the base-emitter junction. Hence, as shown in Fig. 3, the collector current continues to be represented by:

$$I_C = I_{S_C} \exp\left(\frac{q V_{EB}}{kT}\right) \tag{2}$$

where $I_S$ depends on the base-collector voltage. This relation holds as $V_{BE}$ is decreased until injection becomes so low that the collector current is dominated by generation in the base-collector space-charge region.

Base and emitter resistances affect the Gummel plot and cause a deviation from Eq. 2 starting at an $I_C \simeq 0.1$ mA (Fig. 5) [5]. These resistances act to reduce the junction bias, leading to a base-emitter effective voltage of

$$V_{EB_{eff}} = V_{EB} - \Delta V_{EB}$$
$$\Delta V_{EB} = R_B I_B + R_E I_E = (R_B + R_E) I_B + R_E I_C \quad (3)$$

in which $\Delta V_{BE}$ is the voltage drop on $R_B$ and $R_E$.

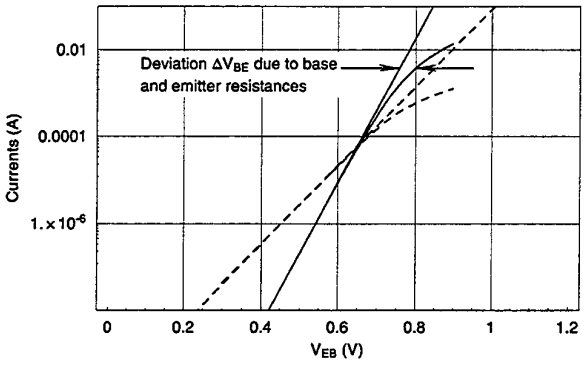


Fig. 5: HBT JP2C Emitter area: 2×30μm² $I_{C_{safe}}$: 30mA $I_{C_{max}}$: 120mA Gummel plot ——— collector current – – – base current

The $h_{fe}$ vs $I_c$ plot is less affected by emitter and base resistive drops because they influence only the base-collector voltage. Underlying device physics can so be investigated by means of this plot (Fig. 6). Use of Eq. 1 and 2 give rise to the dotted line on Fig. 6, showing that base and emitter resistances are the only causes of deviation affecting device behavior up to 10 kA / cm$^2$.

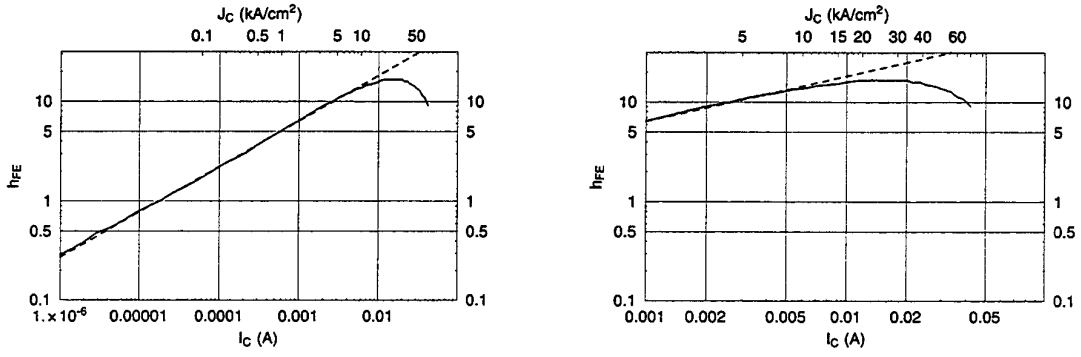


Fig. 6: HBT JP2C Emitter area: 2×30μm² $I_{C_{safe}}$: 30mA $I_{C_{max}}$: 120mA
Differential gain ——— actual $h_{fe}$ – – – extrapolated $h_{fe}$

Emitter resistance is not negligible as can be inferred by the slope of the collector current as function of the collector-emitter voltage in deep saturation conditions (Fig. 2, left). This slope is determined [6] by

the sum of the collector and emitter resistances and its value is of about 16Ω in the sample tested. This value is high enough to induce deep saturation, with a sharp increase in the base current at high collector current densities, observed at $V_{BC} = 0$ (Fig. 7). Non-saturated characteristics can be recovered by biasing the base-collector junction at $V_{BC} = 0.5\ V$, as shown in Fig. 7.

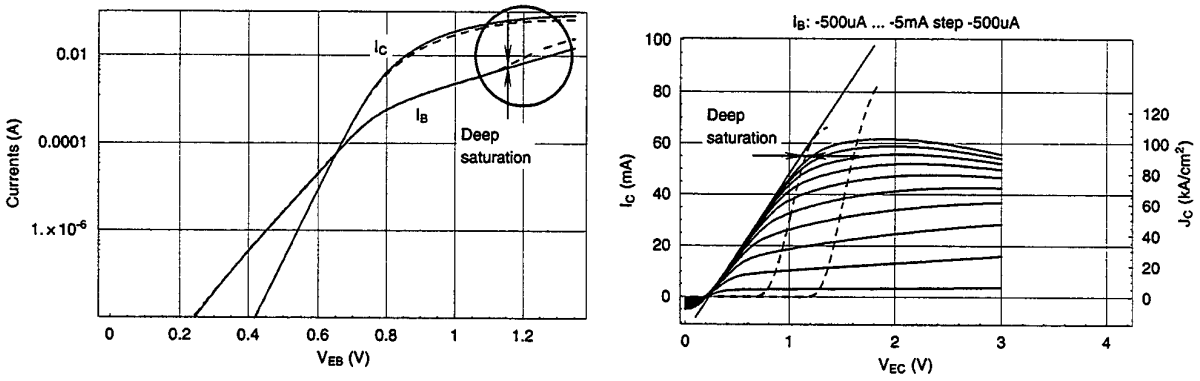


Fig. 7: HBT JP2C Emitter area: 2×30μm² $I_{C_{safe}}$: 30mA $I_{C_{max}}$: 120mA
Left: Gummel plot for $V_{BC} = 0.5\ V$ ——— and for $V_{BC} = 0\ V$ – – –
Right: Common emitter output characteristics

The maximum $\beta$ is 13 at $J_C = 53\,\mathrm{kA/cm^2}$, and the maximum $h_{fe}$ is 17 at $J_C = 20\,\mathrm{kA/cm^2}$, as shown in Fig. 8. Previously reported maximum $\beta$ was 12 at $J_C = 34.8\,\mathrm{kA/cm^2}$ [1].

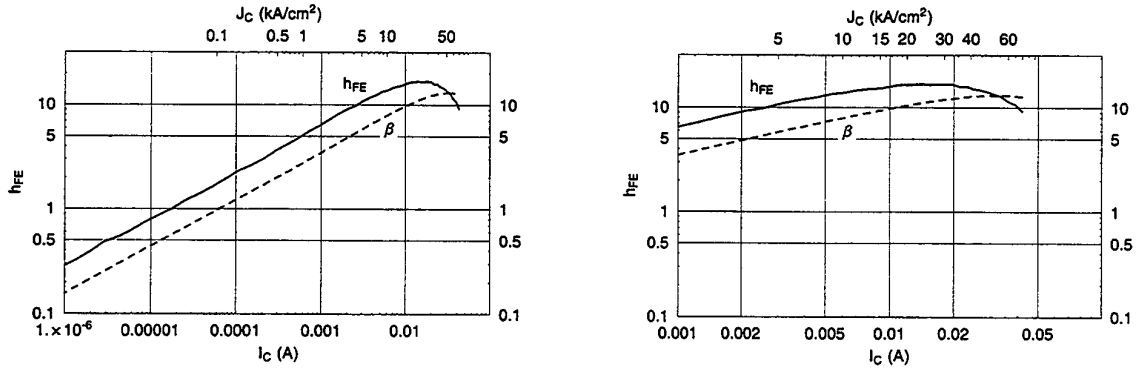


Fig. 8: HBT JP2C Emitter area: 2×30μm² $I_{C_{safe}}$: 30mA $I_{C_{max}}$: 120mA

As can be seen from the forward I-V curve (Fig. 2), the gain increases significantly ($\beta > 20$ and $h_{fe} > 30$) at higher $V_{EC}$. However, the gain compresses rapidly for $J_C > 50\,\mathrm{kA/cm^2}$ due to base push-out, that is a widening of the neutral base in the low doped collector due to the fact that free carriers entering the base-collector space-charge region modify the background charge and affect the electric field. This widening implies a lowering in the small signal current gain, due to the increased neutral base recombina-

tion currents and the short diffusion length of the holes in $In_{0.53}Ga_{0.47}As$, and a degradation of frequency performances. To have an analytic idea of the collector current density needed for approaching base push-out, we can consider the net charge density in the low doped collector region:

$$\rho = qN_A - \frac{J_C}{v_s} \tag{4}$$

where $N_A$ is the acceptor density, $J_C$ is the collector current density, and $v_s$ is hole saturation velocity. With $N_A = 3\times10^{16}\,\mathrm{cm}^{-3}$ and assuming $v_s = 4.5\times10^{6}\,\mathrm{cm}\,s^{-1}$ [4], we have that the neutral collector condition, $\rho = 0$, is reached at $J_C \simeq 22\,\mathrm{kA\,cm}^{-2}$. This condition roughly corresponds to the beginning of base push-out (and actually slightly underestimates it).

These values agrees with the maximum collector current density prior to base push-out from simulations [1] using similar collector doping. Base push-out effects were also seen in frequency measurements were a rapid decrease of $f_T$ and $f_{max}$ was observed for collector currents greater than about 20 $\mathrm{kA/cm}^2$ [1].

Temperature measurements performed on a $2\times10\mu m^2$ sample demonstrates that current gain $\beta$ increases at increasing the temperature at low collector current densities ($J_C < 20$ kA/cm$^2$), where base-emitter space-charge region or surface recombination dominates. At high current densities base push-out occurs and $I_B$, and therefore $\beta$, are dominated by neutral-base recombination; in this region of operation $\beta$ decreases at increasing the temperature, as confirmed by the circled region in Fig. 2, in which the increased device self-heating due to the increased base-collector voltage results in a decrease in $\beta$. This dependence is probably due to the temperature dependence of the hole lifetime in the pushed-out base or of the hole drift saturation velocity.

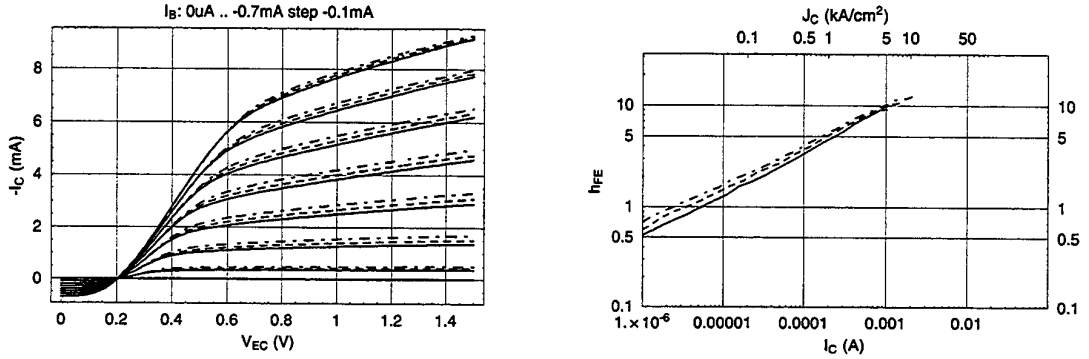


Fig. 9: Preliminary thermal characterization of HBT JP2A Emitter area: $2\times10\mu m^2$ $I_{C_{safe}}$: 10mA $I_{C_{max}}$: 40mA T: 30°, 50° and 70°.
——— 30°C – – – 50°C - - - - 70°C

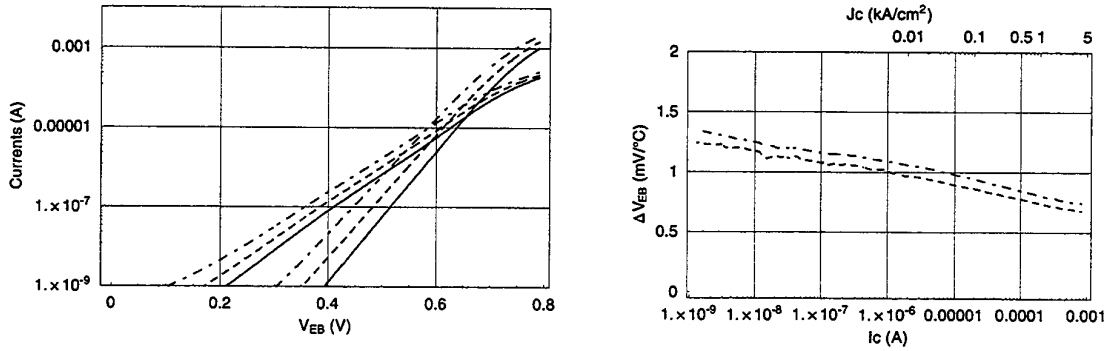


Fig. 10: Base-emitter voltage shift for HBT JP2A Emitter area: $2\times10\mu m^2$ $I_{C_{safe}}$: 10mA $I_{C_{max}}$: 40mA Base temperature: 30°.
Left: Gummel plot ——— 30°C – – – 50°C - - - - 70°C
Right: base-emitter voltage shift Comparative temperatures: – – – 50°C (ΔT=20°C) - - - - 70°C (ΔT=40°C)

In the low collector current region a base-emitter voltage shift of about 1mV/°C is experienced (Fig. 10). The shift is bias dependent due to a lowering of the base ideality factor of about 0.005 $K^{-1}$ (Fig. 11), which affects the slope of $h_{fe}$ at the varying of the temperature (Fig. 9).

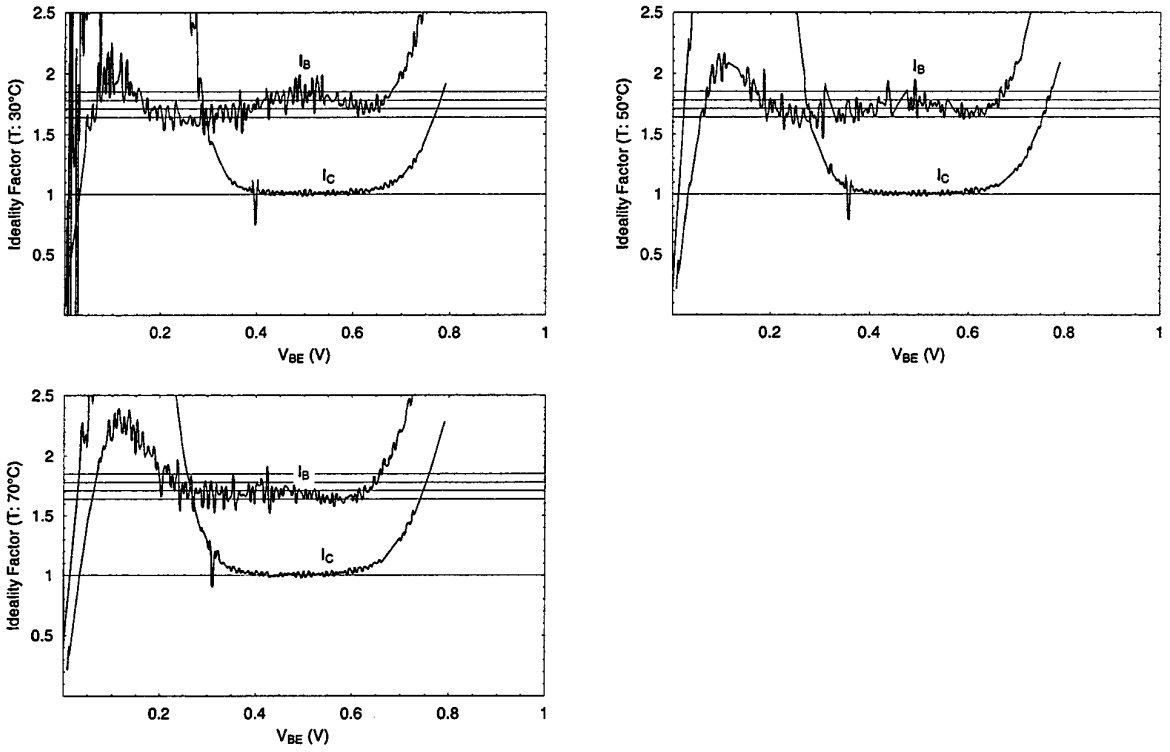


Fig. 11: Base and collector ideality factors at the varying of the temperature on HBT JP2A Emitter area: 2×10μm² $I_{C_{safe}}$: 10mA $I_{C_{max}}$: 40mA

As shown in Fig. 10 both base and collector currents increase at the increasing of the temperature, but for $V_{BE}$ = const, the latter increases more than the former. So we can expect that at a constant base-emitter voltage base current increases at the increases of the temperature, while it has to decrease in constant collector current measurements (that is to say constant emitter current measurements).

# 1.5 Impact Ionization Measurements

## 1.5.1 Theoretical considerations

**In this section the extraction of impact ionization coefficients from multiplication measurements relies upon classical, local field impact ionization equations. Solving these equations in $\alpha_p$ is somewhat complicated and some semplifications have to be made. The aim of this section is to highlight the negligible numerical error introduced by these semplifications. In order to do this, starting from the assumption that ideal ionization coefficients are known, multiplication factors will be calculated according to the known most complete analytical formulation, simplified equations will be applied to $M-1$, and the underlying ionization coefficient $\alpha_p$ will be extracted. The so found coefficient will be found to coincide with the ideal one, implying negligible numerical errors.**

The most straightforward technique for determining impact ionization coefficients in semiconductors is to perform photocurrent multiplication measurements in p-n junctions as a function of the bias voltage. One of the advantages of this technique is the capability to perform measurements of the multiplication factor $M-1$, given by the ratio of the generated to the injected carriers in the region where impact ionization takes place, in presence of pure electron injection, $M_e(V)$, and pure hole injection, $M_h(V)$, in the same device structure and in the same electrical conditions. This capability enables one to overtake the difficulties originated by the fact that electron and hole impact ionization factors come always together in classical, local-field, multiplication expression like [7]

$$M_h = \frac{1}{1-\int_0^{W_c}\alpha_p(x)\exp\left\{-\int_0^x[\alpha_p(y)-\alpha_n(y)]\,dy\right\}dx} \tag{5}$$

$$M_e = \frac{1}{1-\int_0^{W_c}\alpha_n(x)\exp\left\{-\int_x^{W_c}[\alpha_n(y)-\alpha_p(y)]\,dy\right\}dx} \tag{6}$$

and enables one to derive mathematically correct solutions for Eq. 5 and 6 solved in $\alpha_n$ and $\alpha_p$ [8]

$$\alpha_n(E_m) = \frac{E_m}{M_n M_p}\frac{dM_n}{dV} \tag{7}$$

$$\alpha_p(E_m) = \alpha_n(E_m) + E_m\frac{d}{dV}\ln\left(\frac{M_p}{M_n}\right) \tag{8}$$

where $M_n$ and $M_p$ are the electron and hole multiplication values corresponding to a certain value of the base-collector voltage corresponding to a peak electric field value $E_m$. As it will be shown in the following this exact calculation is not necessary in short geometry device structures. In this case secondary impact ionization events are almost absent even at high fields (as can be inferred by the fact that $M-1$ remains close to zero even at high base-collector voltages).

The correlation between $M-1$ and secondary impact ionization events is shown in Fig. 12, left, where the complete integral in Eq. 5 is compared with the equation obtained neglecting the innermost integral (that it is to say secondary impact ionization events). The device parameters listed in Table 1 and the ionization coefficients from Osaka et al. [9] were used. As it can be seen they almost coincide, indicating that secondary impact ionization events are negligible in these type of structures, at these electric fields. In Fig. 12, right, is shown the influence of secondary impact ionization events at three different collector widths, in devices having the same full depleted collector reverse voltage. As it can be seen the influence of secondary impact ionization is greater at the increase of the collector width.

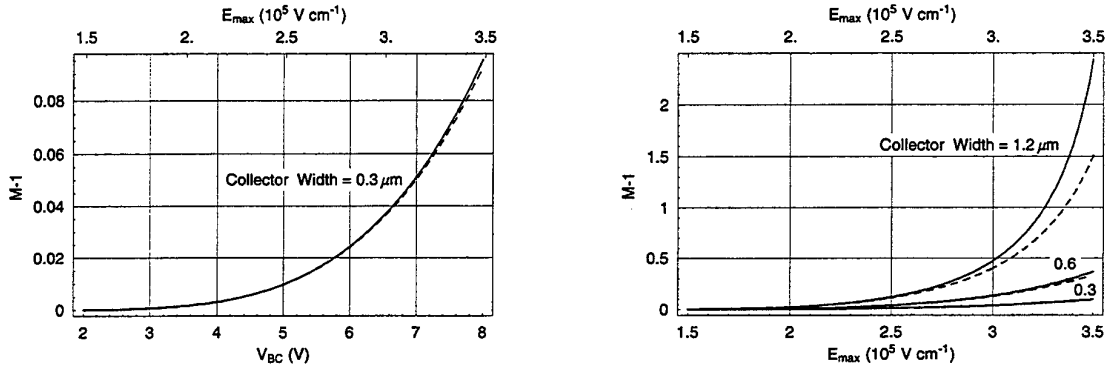


Fig. 12 $M-1$ vs base-collector voltage considering or neglecting secondary impact ionization events.
– – – – Neglecting secondary impact ionizaton events ——— Considering secondary impact ionizaton events

However it has to be stressed that a description of impact ionization by means of ionization coefficients depending only on the local electric field is not completely adequate in thin multiplication regions where a fast varying electric field is present. In devices with thin multiplication lengths nonlocal effects become significant, but a first order correction can be carried out taking into account "dead space" effects. When a carrier is injected at the edge of the depletion region it must travel a finite distance $x_{th}$ in the electric field before it acquires a non-zero carrier ionization threshold energy [10] and can possibly cause ionization. The region between the depletion edge and $x_{th}$ is called "dead space", because in this region the injected carriers can be assumed to have zero ionization probability. Neglecting the high doped regions surrounding the low doped active region the following expression can be given for $x_{th}$ [11]

$$\epsilon_{th} = q \int_0^{x_{th}} E(x)\, dx \tag{9}$$

where $E(x)$ is the electric field profile with the depletion region edge at $x = 0$ and $\epsilon_{th}$ is the threshold energy for the carrier-initiated impact ionization.

For devices having low carrier concentrations and therefore wide active regions, the dead space constitutes a small fraction of the total depletion region and so its effects are negligible. However, for devices with heavy doping or for punch-through devices like that in Fig. 1, the depletion region is narrow and

$x_{th}$ can be significant, so that the injected electrons may travel well past the peak field value before reaching the ionization threshold energy.

It has to be stressed that there is no way to give experimental evidence of dead-space effects when examining data obtained from just one structure, as it is in the present case, and it is necessary to compare measurements on several structures having different depletion-region widths. However there are enough experimental works to trust in the proposed formulation. Assuming $\epsilon_{th}^{e} = 1.84 - 1.02\,y\,(\mathrm{eV})$ for electrons and $\epsilon_{th}^{h} = 1.65 - 0.82\,y\,(\mathrm{eV})$ for holes in $Ga_{1-x}In_xAs_yP_{1-y}$[9] (i.e. $\epsilon_{th}^{e} = 0.82\,\mathrm{eV}$ and $\epsilon_{th}^{h} = 0.83\,\mathrm{eV}$ in $In_{0.53}Ga_{0.47}As$) we can apply Eq. 9 to Eq. 5 and 6, obtaining [11]

$$1 - \frac{1}{M_p}\exp\left[\int_{x_{th}}^{W_c}\alpha_p(x)\,dx - \int_0^{W_c}\alpha_n(x)\,dx\right] = \int_{x_{th}}^{W_c}\alpha_n(x)\exp\left[\int_{x_{th}}^{W_c}(\alpha_p(x') - \alpha_n(x'))\,dx'\right]dx + \left\{\int_0^{x_{th}}\alpha_n(x)\exp\left[-\int_x^{x_{th}}\alpha_n(x')\,dx'\right]dx\right\}\left\{\exp\left[\int_{x_{th}}^{W_c}(\alpha_p(x) - \alpha_n(x))\,dx\right]\right\} \tag{10}$$

where it was assumed $\alpha_p(x) = 0$ in the hole dead-space region ($x<x_{th}$).

A much simpler expression can be found assuming $\alpha_p(x) = \alpha_n(x) = 0$ in the hole dead-space region and considering the innermost integral in Eq. 5 negligible (that is to say neglecting secondary impact ionization events):

$$M_h = \frac{1}{1 - \int_{x_{th}}^{W_c} \alpha_p(x)\, dx} \tag{11}$$

This equation, as it will be shown below, is a good approximation in low multiplication factor conditions, where secondary impact ionization events are negligible. Assuming the active region uniformly doped, with an effective acceptor density of $N_a\,(\mathrm{cm}^{-3})$, and neglecting the low field ($E_{W_c}$) impact ionization coefficient with respect to the high field one ($E_{x_{th}}$), we can solve the previous equation in $\alpha_p(E_{x_{th}})$ obtaining:

$$\alpha_p(E_{x_{th}}) = \frac{1}{\frac{dE_{x_{th}}}{dV}\,\frac{\epsilon_s}{qN_a}} \left( \frac{1}{N_a}\,\frac{dN_a}{dV}\left(1 - \frac{1}{M_h}\right) + \frac{1}{M_h^2}\,\frac{dM_h}{dV} \right) \tag{12}$$

where $N_a$ is assumed to be voltage dependent for taking easily into account the Kirk effect

$$N_a = N_{acc} - \frac{J_c}{q\, v_s} \tag{13}$$

where $N_{acc}$ is the acceptor density, $J_c$ is the collector current density and $v_s$ is the hole drift saturation velocity.

Approximate equations like

$$\alpha_p(E_{\max \text{ or } ave}) = \frac{M_h - 1}{W_c - x_{th}} \tag{14}$$

where $E_{max} = E_{x_{th}}$ and $E_{ave} = (E_{x_{th}} + E_{W_c})/2$ are not as general as Eq. 12.

To prove the accuracy of Eq. 12 and the fact that there is not loss of information going from Eq. 10 to Eq. 11 in the tested structures, we will perform an explicit numerical verification. Assuming the data from Osaka et al. [9] to be approximately right we will consider

$$\alpha_n(E) = 2.19\,10^5\, e^{\frac{-1.12\,10^6}{E}} \tag{15}$$

$$\alpha_p(E) = 3.45\,10^5\, e^{\frac{-1.42\,10^6}{E}} \tag{16}$$

where E is expressed in V/cm. Then using data from Table 1 and adopting Eq. 10, we obtain the best theoretical prediction of $M_h$, where secondary ionization events are duly considered. At this point we come back to $\alpha_p(E)$ using Eq. 12 or Eq. 14, were secondary ionization events and the low field region impact ionization coefficient are completely neglected. The results are shown in Fig. 13. It is clear that only Eq. 12 gives reliable results and that dead space effects are not negligible in the tested structures.

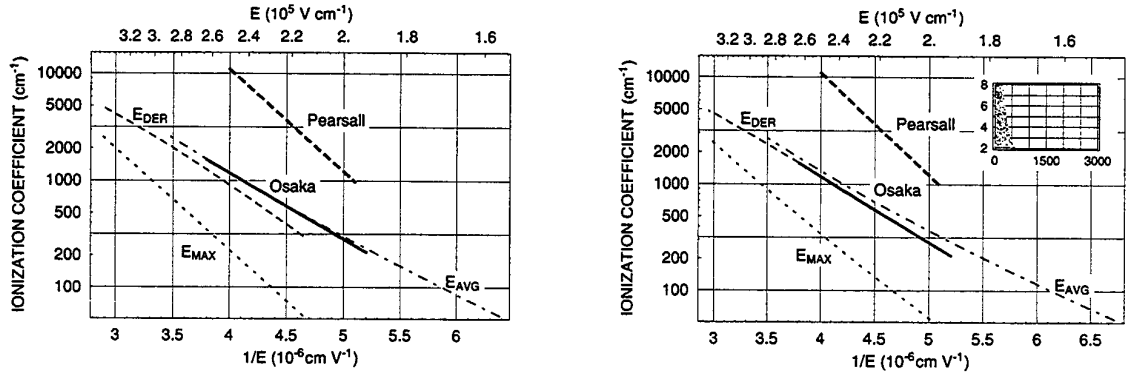


Fig. 13 Thick lines: Referenced hole impact ionization coefficients —— Osaka et al. [9] – – – Pearsall [16]
- — - — - average field — — — derivative - - - - maximum field
In the inset is shown the extension of the dead space region compared with the total collector width
Left: neglecting dead-space effects Right: considering dead-space effects

# 1.6 Impact Ionization Measurements

## 1.6.1 Practical considerations

Preliminary impact ionization measurements were performed adopting a constant emitter current technique at different current levels. This technique is explained in detail in [13], [14] and [15] and its main features are summarized here.

When a pnp transistor is biased in the forward active region the holes injected into the collector are accelerated by the reverse biased base-collector junction electric field. At the increase of the reverse voltage $V_{BC}$, and consequently of the electric field in the space charge region, the holes can gain sufficient energy to create electron-hole pairs by impact ionization. The generated hole are swept toward the collector contact contributing a positive term ($\Delta I_C$) to the total collector current, while the electrons are collected at the base contact, contributing an opposite term ($\Delta I_B = \Delta I_C$) to the base current. The ratio of the hole current $I_C$ coming out of the B-C space charge region to the hole current $I_C'$ injected into that region define the hole multiplication factor $M_h$; consequently the quantity $M_h - 1$ gives the ratio of the current generated by impact ionization to the primary current injected into the B-C space charge region. Of course $\Delta I_B / I_{B0}$, where $I_{B0}$ is the base current that there would be in absence of impact ionization, is grater than $\Delta I_C / I_C'$ by a factor equal to the current gain $\beta$ of the transistor. Conseguently, from an experimental point of view, it is convenient to measure the avalanche current as a change in the base current to enhance the sensitivity of the measurement. The higher the gain the grater the benefits. Thus the multiplication factor can be evaluated as:

$$M_h - 1 = \frac{I_B(V_{BC}) - I_{B0}}{I_C - (I_B(V_{BC}) - I_{B0})} = \frac{\Delta I_B}{I_C - \Delta I_B} \tag{17}$$

Usually $I_{B0}$ is assumed to be independent from base-collector voltage and equal to $I_B|_{V_{BC}=0}$. When Early or self heating effects are not negligible this assumption is false and we have to find a better approximation for $I_{B0}$. Early and self heating effects lead to a decrease in $I_B$ at increasing the base-collector reverse voltage. These effects violate the assumption that the decrease in base current at increasing $V_{BC}$ is mainly due to impact ionization. Kirk effect considered in previous section has no influence on the base current $I_B$ because base push-out does not occur at the emitter current levels used in these experimental impact ionization measurements. However it has an influence on the base-collector space-charge region electric field and this influence has been taken numerically into account in the extraction of the impact ionization coefficient as stated in Eq. 12 and 13. It has to be noted that Eq. 17 holds even for an ionization-free base current $I_{B0}$ dependent on the base-collector voltage and can be rewritten as:

$$M_h - 1 = \frac{I_B(V_{BC}) - I_{B0}(V_{BC})}{I_C - (I_B(V_{BC}) - I_{B0}(V_{BC}))} = \frac{\Delta I_B}{I_C - \Delta I_B} \tag{18}$$

Having a good estimate of $I_{B0}(V_{BC})$ is essential for obtaining a reliable $M_h - 1$, and it is the main cause of error in this kind of measurements. The only exception is when the multiplication is so high that we

can neglect $I_{B0}(V_{BC})$ (or an its estimated value) with respect to $I_B(V_{BC})$. This condition is considered in [15] in relation to self-heating effects, but it is not met in the present case. A good approximation to $I_{B0}(V_{BC})$ can be obtained if base current is mainly due to base-emitter injection or base-emitter recombination. This method, explained in (ref), consist to record the emitter-base voltage ($V_{BE}$) during the impact ionization measurement, sweeping the collector-base voltage ($V_{BC}$) at a fixed emitter current ($I_E$). Because of the Early effect, the base current injected into the emitter decreases at increasing $V_{BC}$, with a decreases in the $V_{BE}$. In the stated hypotesis we have:

$$I_{B0}(V_{BC}) = I_B(V_{BE})\,|_{V_{BC}=0} \tag{19}$$

with $V_{BE}$ function of $V_{BC}$. The main problem with this technique is that it rely on the assumption of negligible thermal effects. This is not true in the tested devices and the strong dependence of the current gain on temperature makes this method useless. An approximate correction, taking into account thermal effects, will be presented afterwards in order to justify the corrections we have used.

Another source of error in the multiplication factor measurements is gived from the non negligible base-collector junction reverse current ($I_{CBO}$) at high $V_{BC}$. The presence of $I_{CBO}$ decrease further the $I_B$, with a conseguent overestimation (mainly at high $V_{BC}$) of the base current variation due to impact ionization. From the theoretical point of view, a slightly more accurate equation can be obtained by assuming that the base-collector junction reverse current originates mostly from the region outside the device active area. If this is true a principle of superimposition can be used and Eq. 18 can be modified as:

$$\Delta I_B(V_{BC}) = I_B(V_{BC}) - I_{B0}(V_{BC}) + I_{CBO} \qquad I_{Cc} = I_C - I_{CBO}$$
$$M_h - 1 = \frac{\Delta I_B}{I_{Cc} - \Delta I_B} \tag{20}$$

### 1.6.2 Measurements

From the experimental point of view emitter current levels have to be chosen so that: 1. base-collector reverse current $I_{CBO}$ is small compared to impact ionization current and 2. thermal effects are negligible. These two conditions are partially conflicting in this kind of devices, characterized by high base-collector reverse current.

In this work measurements with an emitter current density ranging from 1 to 4 kA cm$^{-2}$ were performed on different device geometries, mainly $2\times10\,\mu m^2$ and $5\times10\,\mu m^2$ emitter-geometry devices.

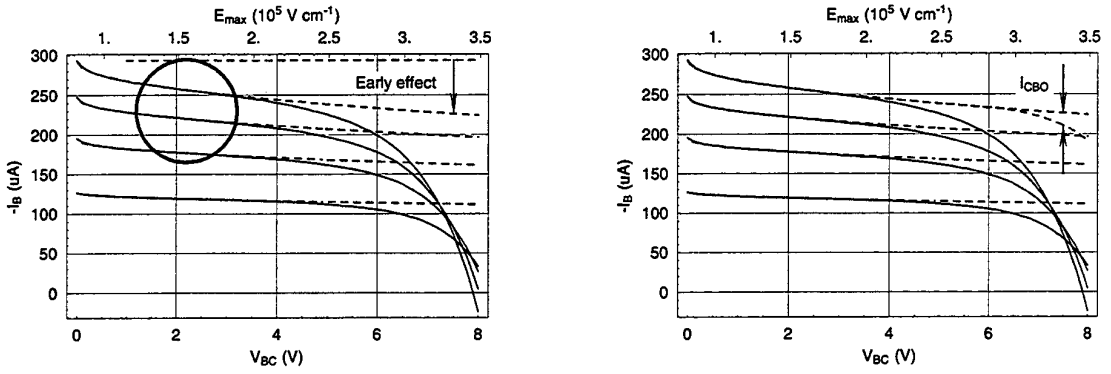


Fig. 14: Impact ionization measurements for HBT JP3A Emitter area: 5×10μm² $I_{C_{safe}}$: 25mA $I_{C_{max}}$: 100mA $I_E$: 0.5mA ... 2.0mA step 0.5mA

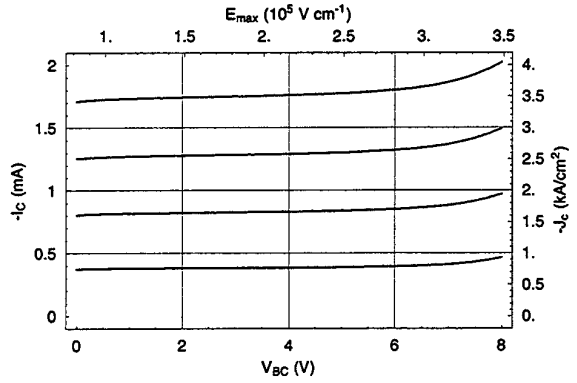


Fig. 15: Impact ionization measurements for HBT JP3A Emitter area: 5×10μm² $I_{C_{safe}}$: 25mA $I_{C_{max}}$: 100mA $I_E$: 0.5mA ... 2.0mA step 0.5mA

As previously stated hole impact-ionization coefficient extraction measurements rely on the assumption that the decrease of base current at increasing $V_{BC}$ (see Fig. 14, left) is mainly due to impact ionization. In the samples that we have measured this is not strictly true. Early and thermal effects are heavily present, causing an $I_B$ bending even at low values in $V_{BC}$ (see the circled region in Fig. 14, left). At the increase of $V_{BC}$ we have another source of error due to a non negligible $I_{CBO}$(Fig. 14, right). In past papers dealing with impact ionization measurements on more usual materials $I_{CBO}$ was at least four orders of magnitude smaller than $\Delta I_B$ [13]. In the present case $I_{CBO}$ is of the same order of magnitude of $\Delta I_B$ (Fig. 14, right, assuming superimposition), possibly leading to an overestimation of the $\Delta I_B$ itself and of the impact ionization coefficient $\alpha_p$. Thermal effects made actual isothermal impact ionization measurements not feasible and they prevented base-emitter voltage impact ionization measurements. .

All these effects prevent us from performing strict measurements of $\alpha_p$. Other effects such as resistive drops or bendings in the base current at low $V_{BC}$ are at the moment second-order error sources. The

bending of $I_B$ at low $V_{CB}$ appears to be caused by base width modulation. At the moment we do not quantitatively know if the partially depleted collector influence on base modulation is sufficient to explain this phenomenon. Slight quasi-saturation effects are another possible explanation for the shown rise in $I_B$.

We can perform a rough evaluation of the ionization coefficient taking partially into account the base-collector reverse current, Early and thermal effects. The method is not strictly correct, but the results (Fig. 16) are in good agreement with data obtained by Osaka et al. by photomultiplication measurements [9].

We have assumed that the Early and thermal effects give rise to an almost linear (actually square rooted) decrease in $I_B$ at the increase of $V_{BC}$, as shown in Fig. 14. $I_{CBO}$ is simply subtracted from the result assuming the validity of superimposition. $\Delta I_B(V_{BC})$ and $M_h - 1$ are computed as stated in Eq. 20. Eq. 12 is applied to the data so obtained.

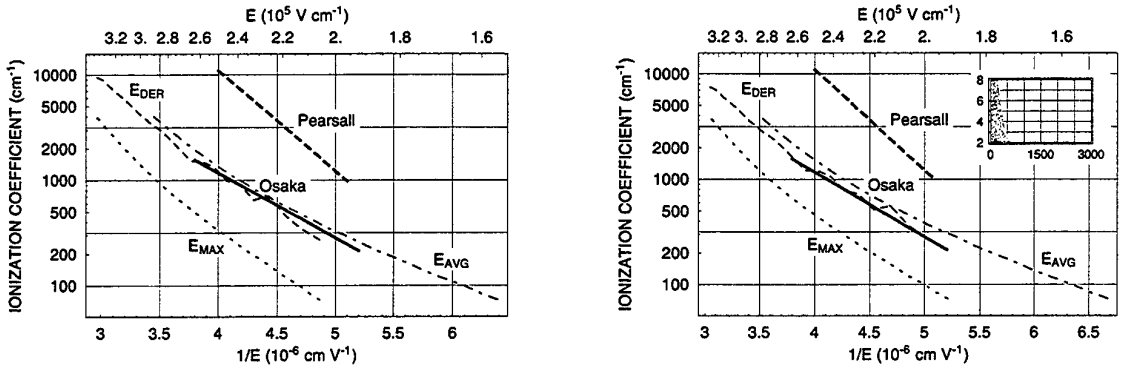


Fig. 16: Hole impact ionization coefficient for HBT JP3A Emitter area: 5×10μm² $I_{C_{safe}}$: 25mA $I_{C_{max}}$: 100mA
left: neglecting dead space and Kirk effects right: taking into account dead space and Kirk effects
In the inset is shown the extension of the dead space region compared with the total collector width
——— our results —·—· average field - - - - - maximum field
——— Osaka et al. [9] ——— Pearsall [16]

As shown in Fig. 17, right, neglecting $I_{CBO}$ in $\Delta I_{B0}$ leads to a greater spread (not dramatic) in the ionization coefficient at the varying of the current level with respect to the case in which it is considered (Fig. 17, left). This support the fact that the newly introduced term reduces measurement errors. From Fig. 17, left and right, we can also infer that the uncertainty introduced by the Early and thermal corrective term prevents us from extracting the M-1 multiplicative term at voltages below about 4V. We are so prevented from doing low field impact ionization coefficient extraction.

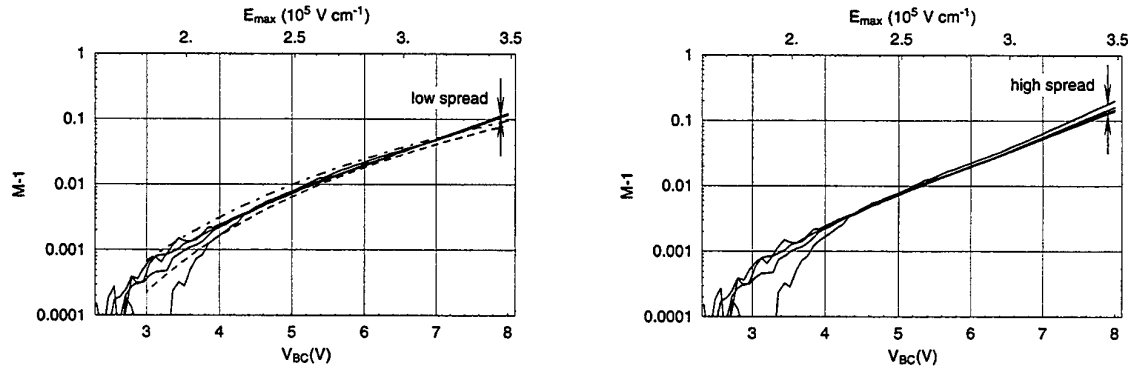


Fig. 17: $M-1$ under different approximations for HBT JP3A Emitter area: 5×10μm² $I_{C_{safe}}$: 25mA $I_{C_{max}}$: 100mA
left: ——— $M-1$ considering $I_{CBO}$ — - — - Theoretical $M-1$ without dead-space and Kirk effect
— — — Theoretical $M-1$ taking into account dead-space but neglecting Kirk effect (data calculated using as reference Osaka et al. [9])
right: ——— $M-1$ neglecting $I_{CBO}$

### 1.6.3 Early and thermal effect corrections

In these devices, at these current levels, base-emitter space charge recombination is the main term of base current. We are in the hypothesis stated in [15] for applying Eq.19, but thermal effects vanish our efforts. As shown in Fig. 19, left, actual base current is greater than the predicted one at the same base-emitter voltage with the base-collector junction short-circuited even at low values in $V_{BC}$.

This behavior is incompatible with the presence of main neutral-base recombination currents and can be explained by the introduction of non-negligible thermal effects. We can come back to an approximated version of the actual base current behavior by assuming a constant thermal resistance (1200 °C/W) and a voltage shift in the Gummel base current plot proportional to device temperature (1 mV/°C as derived from Fig. 9 ). The approximation is poor for correction term purposes and is useful only in proving the correctness of the hypotheses. The method followed is analogous to [17], but only the added power dissipation with respect to the Gummel plot is taken into account:

$$\Delta P_{DC} = \Delta I_E V_{BE} + I_C V_{CE} \quad \text{where } \Delta I_E = I_{E_{\text{eff}}} - I_{E_{\text{Gml}}} \tag{21}$$

$$I_{B_{\text{eff}}}(V_{BE}) = I_{B_{\text{Gml}}}(V_{BE} + R_{\text{th}} \Delta P_{DC} v_{\text{shft}}) \tag{22}$$

The reported thermal resistance agrees well with the value found by S. S. H. Hsu [18] on the same kind of devices, with the same geometry ($5 \times 10\,\mu m^2$). The main difference is in the power levels used: up to 18 mW in our case, between 120 mW and 180 mW in the reported paper.

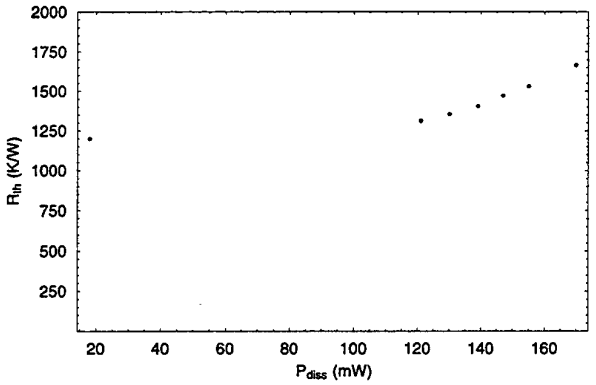


Fig. 18: Measured [18] thermal resistance at a constant base current ($I_B = 3\,mA$) for an HBT JP3A Emitter area: 5×10μm² $I_{C_{safe}}$: 25mA $I_{C_{max}}$: 100mA. Our data are summarized in the left-most point.

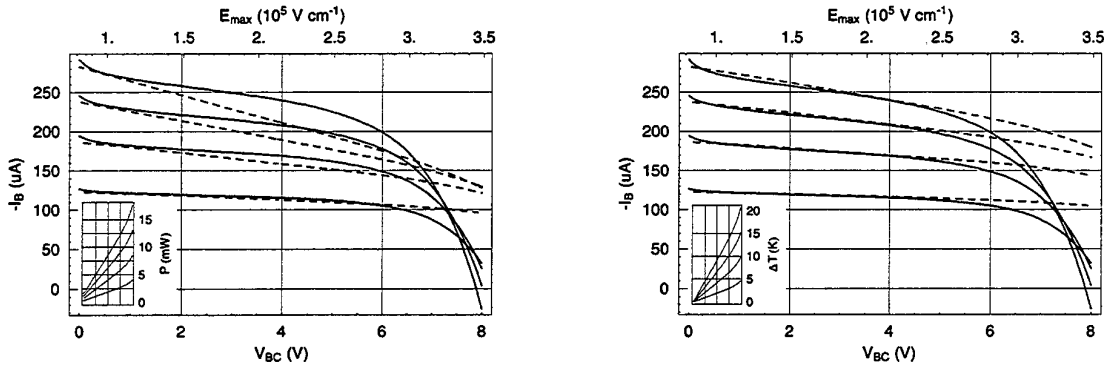


Fig. 19: Impact ionization measurement for HBT JP3A
Emitter area: 5×10μm² $I_{C_{safe}}$: 25mA $I_{C_{max}}$: 100mA $I_E$: 0.5mA ... 2.0mA step 0.5mA
Left: superimposed on the $I_B$ curves are shown the base currents obtained from the Gummel plot (with $V_{CB} = 0$) at the measured $V_{EB}$.
Right: superimposed on the $I_B$ curves are shown the base currents obtained from the Gummel plot (with $V_{CB} = 0$) at the measured $V_{EB}$ taking into account thermal effects.

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# Chapter 2

# Study of Hot Carrier Phenomena in Heterojunction Devices by Means of Pulsed Measurements

*Abstract*– In this section we summarize the results obtained by means of the Transmission Line Pulsed testing system on commercially available GaAs MESFETs, on GaAs-based and InP-based HEMTs and on laboratory prototypes.

Results can be summarized as follows: (a) we demonstrate that, due to the non negligible influence of thermal effects on breakdown characteristics, and to the presence of unstable portions of I-V curves of the devices, TLP is the only technique which enables a realistic evaluation of on-state breakdown characteristics of power devices; (b) by measuring non-destructively the on-state breakdown curves up to gate current density levels never reached in the literature (i.e. 30 mA/mm), we noticed that at least in the tested devices breakdown is triggered by a self-regenerative effect due to a parasitic bipolar action and is quenched by high injection and thermal effects occurring at high drain currents; (c) this analysis of on-state breakdown mechanisms is confirmed by Monte Carlo simulations.

On the basis of the experimental observations, an equivalent circuit model of breakdown suitable for circuit SPICE-like simulations has been developed.

# 2.1 Introduction

Field effect transistors based on III-V semiconductor compounds have excellent high frequency behavior, but reduced safe operating areas. This fact has strongly increased the interest on on-state and off-state breakdown phenomena.

In particular, despite a fairly large number of published studies, there is still no general agreement on the definition of on-state breakdown. The principal problem is that standard DC and pulsed measurements of on-state breakdown in power MESFETs and HEMTs are hindered by thermal effects and degradation, and by the risk of burn-out.

Transmission Line Pulsed techniques [1] appear the most promising tool for non-destructive experimental evaluation of actual breakdown phenomena.

## 2.1.1 TLP Breakdown Measurement Set-Up

The TLP system (extensively described in the first report [1]) generates a square current pulse with fast, sub-ns, rise time. The pulses are obtained by discharging a coaxial line of known length and impedance (Z) over a partially matched load. The line is charged at a prefixed voltage by the use of a high voltage supply and a high value resistor (R>>Z). When the mercury switch is closed, the coaxial line behaves like an ideal square wave voltage pulse generator. The width of the pulse is equal to twice the transmission time of the line, the amplitude is the same of the pre-charging voltage supply value (Vdd), the pulse generator series resistor is equal to the line characteristic impedance. Therefore, by changing the length of the line, pulses of different width can be generated (our system can generate 100ns and 500ns pulses).

Since the load is made by the parallel combination of a matching load (Z) and of the series of the Device Under Test with a high value resistor, the matching is only partially achieved and a pulse reflection can occur. To alleviate this effect the series of a high voltage fast turn-on Schottky diode and a matching resistor (Z) is required at the input of the line (see Fig. 1). In the same figure the actual positions of voltage and current probes are also shown.

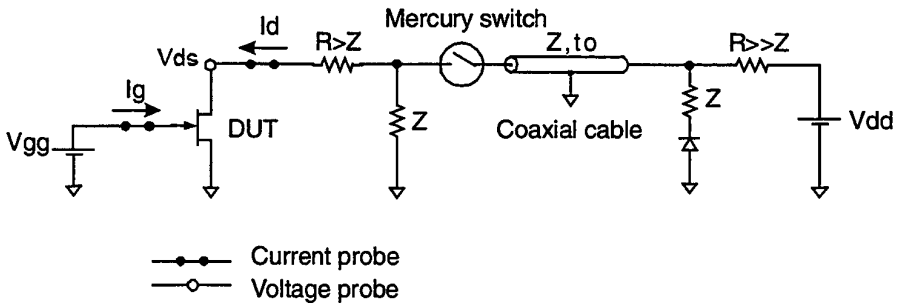


Figure 1: Schematic of the TLP measurement set-up.

## 2.2 Samples Description

The tested devices are FETs and HEMTs based on GaAs and InP. All these devices are strongly affected by impact-ionization and hot carrier phenomena. We have performed TLP measurements on different kinds of devices in order to identify the influence of materials, geometry and technologies on on-state breakdown characteristics.

First we have tested some GaAs MESFETs such as Mitsubishi MGF1601B and Mitsubishi MGF1403.

**Mitsubishi MGF1601B** devices are medium Power GaAs MESFETs with a N-channel Schottky gate and are designed for use in S to X band amplifier and oscillator. They have a maximum total power dissipation of 1.2W (at Tc=25°C) and a thermal resistance (channel to ambient, measured by $\Delta V\gamma$ method [2]) of 125 °C/W; they presented a saturated drain current Idss of 150-250mA and a gate to drain V(br)gdo and gate to source V(br)gso breakdown voltage of –8V (at Ta=25°C at Ig=-0.2 mA).

**Mitsubishi MGF1403** devices are low-noise GaAs MESFETs with an N-channel Schottky gate and are designed for use in S- to Ku- band amplifiers. They have a maximum total power dissipation of 240mW and a thermal resistance (channel to ambient, measured by $\Delta V\gamma$ method) of 625 °C/W; they present a saturated drain current Idss of 15-80mA and a gate to drain V(br)gdo and gate to source V(br)gso breakdown voltage of –6V (at Ta=25°C and Ig = -0.1 mA).

Then we have measured some GaAs HEMTs: Toshiba S8902, Mitsubishi MGF4317D and some laboratory prototypes.

**Toshiba S8902** devices are depletion mode AlGaAs/GaAs microwave HEMTs characterized by a recess gate length Lg=0.3μm and gate width W=200μm, and by gate-to-source and gate-to-drain contact spacing Lgs=0.5μm and Lgd=1.5μm, respectively. The heterojunction structure has been derived by SEM and TEM observations. It is characterized by an AlGaAs layer, ≅30nm thick, on the undoped GaAs layer, ≅350nm thick. An AlGaAs/GaAs (approximately 30nm thick) superlattice buffer is used for separating the active device from the semi-insulating substrate. Devices have recessed Al/Ti gates and an n+ GaAs cap layer, which is approximately 80nm thick and extends from the gate edge to the ohmic contact. They have a maximum total power dissipation of 150mW and a thermal resistance (channel to ambient, measured by $\Delta V\gamma$ method) of 500 °C/W; they present a saturated drain current Idss of 10-50mA.

**Mitsubishi MGF4317D** devices are super-low-noise pseudomorphic HEMTs designed for use in X to K band amplifiers. They have a maximum total power dissipation of 50mW and a thermal resistance (channel to ambient, measured by $\Delta V\gamma$ method) of 625 °C/W; they present a saturated drain current Idss of 10-60mA and a gate to drain V(br)gdo and a worst-case gate to source V(br)gso breakdown voltage of –3V (at Ta=25°C and Ig=-0.1 mA).

**Laboratory Prototypes** are AlGaAs/InGaAs pseudomorphic HEMTs built from epitaxial layer grown by molecular beam epitaxy (MBE) [3]. Their structure consists (from surface to substrate) of a GaAs cap, a Si-doped $Al_{0.2}Ga_{0.8}As$ donor layer, an undoped $Al_{0.2}Ga_{0.8}As$ channel layer, an undoped spacer, a doped

$Al_{0.2}Ga_{0.8}As$ donor layer, an undoped $Al_{0.2}Ga_{0.8}As$ barrier layer, and an undoped GaAs buffer (with superlattice) grown on semi-insulating GaAs substrate. A T-shaped recessed gate with gate length Lg=0.25μm is adopted. Gate-drain distance Lgd, measured from contact edges is 2.1μm; gate-source distance Lgs, is 1.3μm; gate width, W, was varied from 80μm to 240μm. To avoid metal/semiconductor interdiffusion barrier is chosen for the gate metallization. Alloyed AuGeNi ohmic contacts were used for source and drain. Devices are passivated using SiN. Vbr(gdo) with source floating is -8.5 V at Ig = -50 μA.

Finally, we have tested an InP HEMT technology fabricated by HRL Laboratories (formerly Hughes Research Laboratories).

**HRL** devices are AlInAs/GaInAs/InP HEMTs with a composite channel, fabricated by HRL (formerly Hughes Research Laboratories) to study the effects of channel quantization on the electrical characteristics [4]. The components measured have a thickness of the $Ga_{0.47}In_{0.53}As$ layer in the channel of 50Å and a gate length Lg of 0.5μm. Vbr(gdo) with source floating is -9 V with Ig = -50 μA.

The main features of the tested devices are summarized in Table 1

| Supplier, type | Technology, gate length Lg, and width, Wg | Maximum drain current, Idss | Maximum drain voltage Vds | Gate-drain breakdown voltage V(br)gdo | Thermal resistance Rth | Maximum total power dissipation |
|---|---|---|---|---|---|---|
| Mitsubishi MGF1601B | GaAs MESFET | 250 mA | 9 V | -8 V (@Is=0, Ig=-0.2 mA) | 125 °C/W | 1.2 W |
| Mitsubishi MGF1403 | GaAs MESFET | 80 mA | 4 V (Vgd) | -6 V (@Is=0, Ig= -0.1 mA) | 625 °C/W | 0.24 W |
| Toshiba S8902 | AlGaAs/GaAs HEMTs Lg=0.3 μm Wg=200 μm | 50 mA | 4 V | not available | 500 °C/W | 0.15 W |
| Mitsubishi MGF4317D | pseudomorphic HEMTs Lg=0.25 μm Wg=200 μm | 60 mA | 4 V | -3 V (@Is=0, Ig=-0.1 mA, worst case) | 625 °C/W | 0.05 W |
| laboratory prototypes | pseudomorphic HEMTs Lg=0.25 μm Wg=50 μm | 25 mA | 8 V | -8.5 V (@Is=0, Ig= 50 μA) | 125 °C/W | not available |
| HRL Laboratories prototypes | InP HEMTs, lattice-matched Lg=0.5 μm Wg=50 μm | 90 mA | 2 V | -9 V (@Is=0, Ig= 50 μA) | not available | not available |

Table 1: Schematic description and typical values of the main electrical parameters of the GaAs MESFETs and GaAs-based and InP-based HEMT's submitted to tests.

# 2.3 Breakdown Measurement Techniques

Breakdown has been identified by the locus of bias condition where burnout is triggered [5], or where a sudden increase in output conductance takes place [6]. Starting from the work of K. Hui et al. [7], however, measurement of the excess gate current Ig have been used to identify quantitatively the on-state breakdown voltage (BVds) of MESFETs and HEMTs, which is usually defined as the drain-source voltage Vds corresponding to a gate current density of 1mA/mm.

The aim of this section is to show the correlation between the BVon vs Id curves and the well-known bell shape (Ig vs Vgs) measurements. The former is obtained by injecting a constant current Ig in the gate and driving the drain with an increasing current [8]. In the latter the device under test is driven by drain and gate voltage generators.

The breakdown voltage BVds, measured at constant gate current, has a non-monotonic behavior as a function of Id (see Figure 2, left). This is a direct consequence of the similar trend ("bell-shape") shown by the Ig vs Vgs characteristics, see Figure 2, right, and is due to the decrease in gate-drain electric field which take place at high device currents.

Figure 2 shows the output characteristics of a 50μm wide InAlAs/InGaAs HEMT. The characteristics have been truncated at a gate current density of 0.2 mA/mm using as a boundary the BVds-Id curve at Ig=-10μA (solid line).

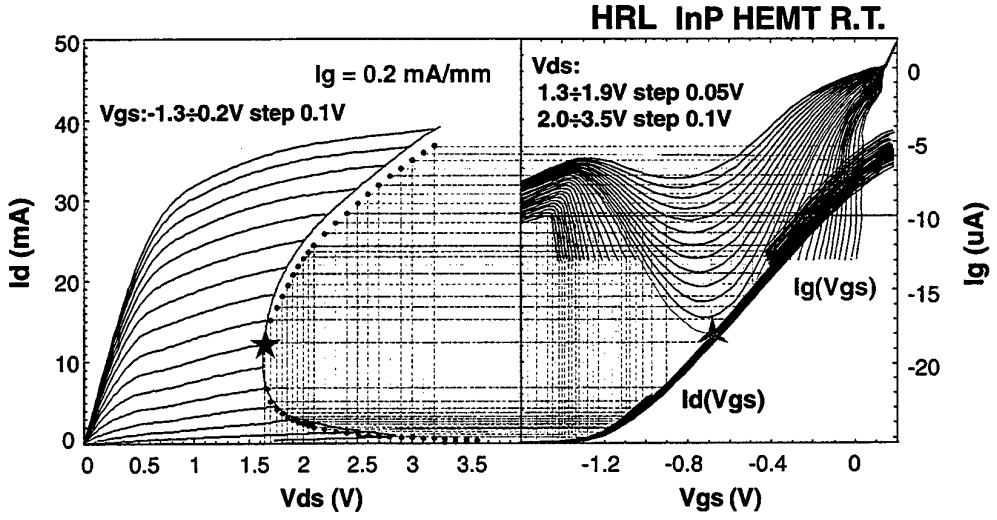


Figure 2: Left: Id vs Vds in tested HRL InP.based HEMTs. These devices have an In0.53Ga0.47As channel layer thickness of 50Å and a gate length Lg of 0.5μm. Curves are truncated by Id-BVds locus at constant Ig=-10μA. Dots are points at Ig=-10μA extrapolated from Ig vs Vgs curves (right). DC measurements have been carried out by HP 4145B Semiconductor Analyzer.

The same curve can be obtained from the measurements of the Ig vs Vgs and Id vs Vds characteristics using a graphical method. Being fairly complicated, this method is not practical, and is reported here only

to describe the correlation between Id-BVds (@ Ig/W=constant) measurements and the Ig vs Vgs curve.

First, the intersection of the Ig=constant horizontal line with the Ig(Vgs) curves, measured for different Vds values, provides a series of Vgs values which can be read on the X-axis of Fig. 2, right. For each Vds value, the corresponding Id value is reported on the output characteristics (the dots in Fig. 2, left). This series of values represent the Id(Vgs, Vds) points corresponding to a constant gate current (density), Id vs BVds (@ Ig=constant). The maximum in gate current (vs Vgs, marked by a 'diamond' symbol in Fig. 2, right) obviously corresponds to the minimum BVds (vs Id) value (marked by a 'star' symbol in Figure 2, left). The position of this minimum and the slope of the BVds-Id curve influences the choice of the load line. The position of the maximum of the Ig vs Vgs curve is therefore crucial for device power applications.

The differences between the direct measurements, solid line in Fig. 2 and the interpolated values, shown as dots in the same figure, are due to slight thermal effects occurring at high currents, which will be discussed in the following.

### 2.3.1 Thermal Effects on Breakdown Measurement

DC measurements of on state breakdown are remarkably affected by thermal effects which, especially in power devices, may lead to an incorrect evaluation of the breakdown voltage. An example is shown in Figure 3, which reports the output characteristics and on-state breakdown characteristics at Ig/W=0.6 mA/mm obtained on a commercially-available medium power (1.2W), S to X band GaAs MESFET (Mitsubishi MGF1601) in DC and pulsed conditions.

This device is characterized by a thermal resistance of 150 °C/W, which corresponds to a Tch=320°C at the peak Id and Vds values applied (Vds=10V, Id=200mA). The thermal resistance was measured by means of measurements of the gate-drain diode knee voltage Vγ, after calibrating the Vg (at Igd= constant) dependence on channel temperature [2].

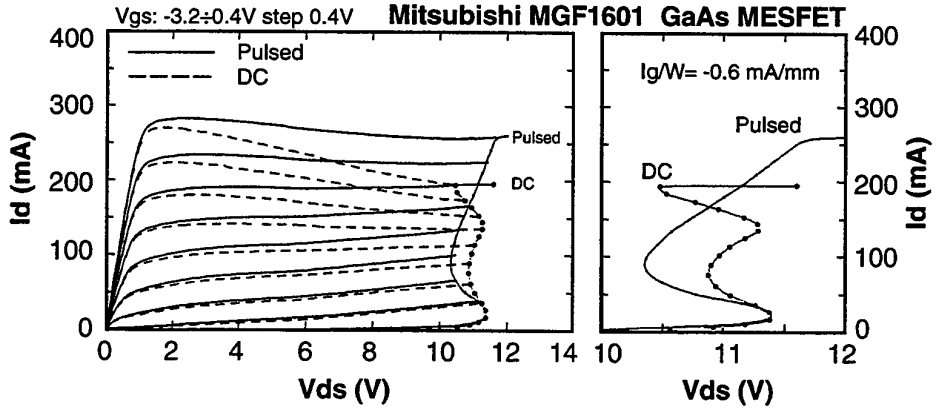


Figure 3: Left: pulsed and DC Id vs Vds characteristics in the tested GaAs MESFETs (Mitsubishi MGF1601). The boundaries at the extreme right represent the Id-BVds loci at constant Ig=-300μA (Ig/W = 0.6mA/mm), extrapolated from the Ig vs Vgs characteristics (not shown). Right: pulsed and DC Id-BVds locus at constant Ig=-300μA measured as in [8]. DC and pulsed characteristics have been measured by means of HP4142. The duty cycle of pulsed measurements is 1% (1ms/100ms).

A remarkable decrease in Id is observed at high Vds during DC measurements due to thermal effects. The breakdown curve deviates from the usual trend [8], which can be recovered only if pulsed measurements are adopted. By looking at Figure 3, right, we can notice that the DC on-state breakdown curve corresponds to the pulsed one only in the pinch-off region, ID < 25 mA, where device self-heating is negligible. When the channel is opened, 25 mA < ID < 150 mA, the increase in channel temperature causes a decrease in impact-ionization, so that the DC breakdown voltage is larger than the one measured with 1 ms pulses, see Fig. 3, right. At very high drain currents, ID > 150 mA, the derivative of the $I_D(V_{DS})$ DC curve changes, and the breakdown voltage starts to decrease at increasing the drain current. The deviation is due to thermal effects which lead to enhanced thermionic field emission of electrons over the gate Schottky barrier at high currents, see the -0.5V < Vgs < 0.4V portion of the $I_G(V_{GS})$ curve in Figure 4. Since thermal effects are due to the device self heating, the region of the characteristics close to pinch-off (Vgs < -3V) is unaffected.

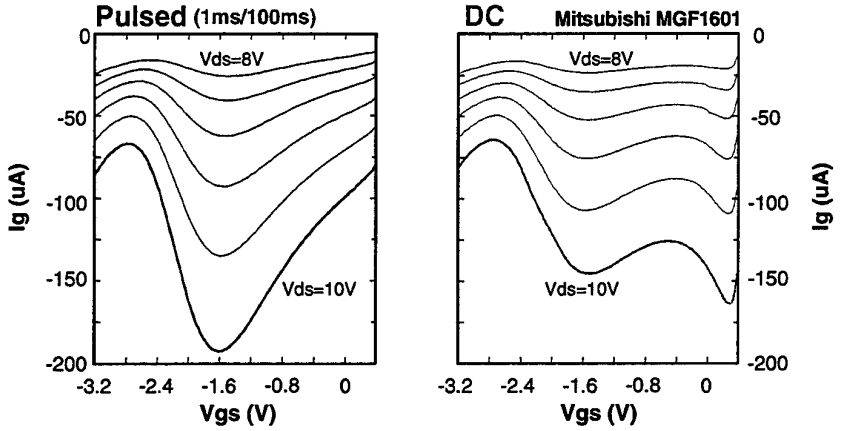


Figure 4: Ig vs Vgs curves of the tested GaAs MESFET (Mitsubishi MGF1601B) measured in pulsed (left) and DC (right) conditions.

When a non-negligible increase in channel temperature due to power dissipation is present (i.e. when DC measurements at high Vds and Vgs are carried out), impact ionization is decreased; nevertheless, as shown in Fig. 4, the gate reverse current may increase due to the increase in thermionic emission of electrons over the gate Schottky barrier [9], possibly leading to an underestimation of the breakdown voltage. If pulsed measurements are adopted, self-heating and therefore thermal effects can be strongly reduced, leading to a more correct evaluation of the breakdown characteristics (Fig. 3, right).

A pulse duration of 1 millisecond, however, is still too long, and thermal effects can not be avoided. Voltage pulse generators, on the other hand, do not allow one to control the device current during the pulse, so that the measurement is often destructive. Moreover, it is difficult to find generators capable of producing sufficiently large voltage pulses with high currents. For these reasons, we have adopted the previously described current pulse testing system based on a charged transmission line.

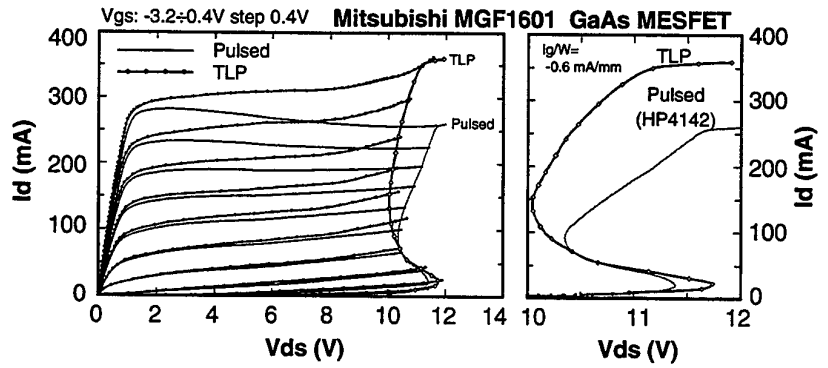


Figure 5: Left: pulsed and TLP Id vs Vds in the tested GaAs MESFETs (Mitsubishi MGF1601). Curves are truncated by the Id-BVds locus at constant Ig=-300μA, extrapolated from the Ig vs Vgs characteristics (not shown). Right: pulsed and TLP Id-BVds locus at constant Ig=-300μA measured as in [8].

Figure 5 compares pulsed voltage and TLP measurements (with a pulse length of 500ns), and demonstrates that pulsed Id vs Vds curves with a 1ms pulse width and a 1% duty cycle are not completely self-heating-free. Therefore a pulse width of 1ms provides a reduction but not a complete elimination of thermal effects.

Figure 6 shows the comparison between DC, pulsed and TLP measurements of the Id and Ig vs Vds characteristics of a Mitsubishi MGF 1601 GaAs MESFET for a Vgs value (Vgs=-1.6V) close to the maximum of impact ionization (see Figure 4): when self-heating effects are reduced, the drain current increases since the lower temperature corresponds to improved carrier transport properties; at the same time, impact ionization efficiency increases. As a consequence, the gate current Ig, due to impact-ionization, increases in absolute value when the 100 ns TLP pulses are adopted with respect to 1 ns pulses, or DC measurements (see Fig. 6). DC, pulsed and TLP measurements of the Id-BVds locus at constant Ig=-300μA are reported in Figure 7.

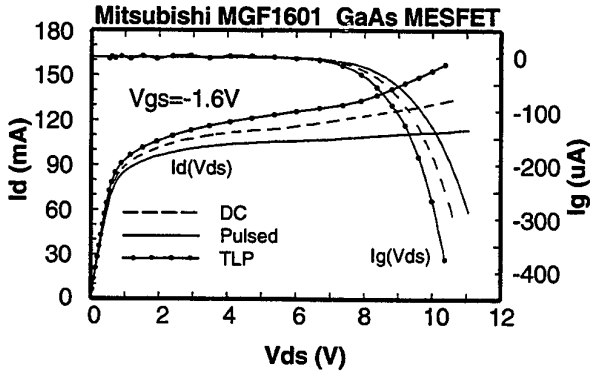


Figure 6: DC, pulsed and TLP Id vs Vds and Ig vs Vds in the tested GaAs MESFETs. The chosen Vgs value corresponds to the maximum of impact ionization.

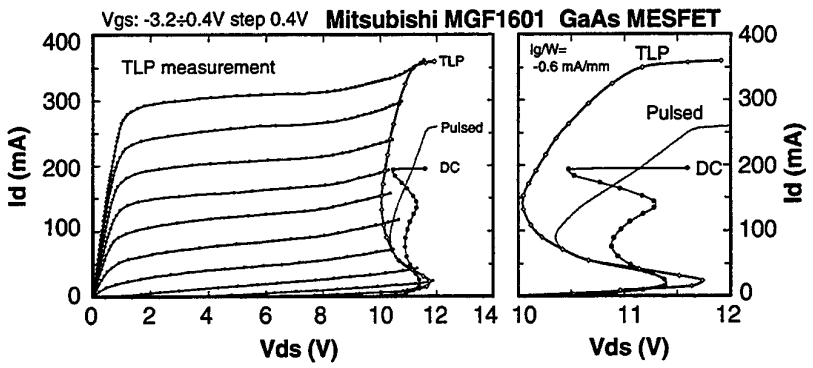


Figure 7: Left:TLP Id vs Vds in the tested GaAs MESFETs. Id curves are truncated by the Id-BVds locus at constant Ig=-300μA, extrapolated from the Ig vs Vgs characteristics (not shown). TLP, pulsed and DC Id-BVds locus at constant Ig=-300μA measured as in [8] (right) are also depicted.

A remarkable difference between the three breakdown curves is evident. In DC conditions the breakdown curve shows a first snap-back at Id≈20mA, which corresponds to the transition from off-state breakdown (initiated by tunneling or tunneling-assisted thermionic emission, [9]) to on state breakdown (impact-ionization limited). Then, at Id≈150mA, the DC characteristic snaps back again due to thermally-activated gate reverse currents, finally, at Id≈200mA, the on-state breakdown ( = constant Ig current) DC curve suddenly moves to very high Vds values due to the forward biasing of the gate Schottky junction (the knee voltage of this diode is lower at higher temperature; the forward gate current partially compensates impact-ionization current, thus leading to an apparent increase in breakdown voltage: compare Fig. 7 with Fig. 8, where Ig vs Vgs characteristics are shown). The 1 ms-pulsed and TLP curves are not affected by these parasitic phenomena, and present a smooth behavior. Nevertheless, we can clearly see that the presence of thermal effects which reduce impact-ionization leads to an overestimation of the BVds-on breakdown voltage at high currents in DC and 1 ms-pulsed conditions with respect to TLP ones, see Fig. 7.

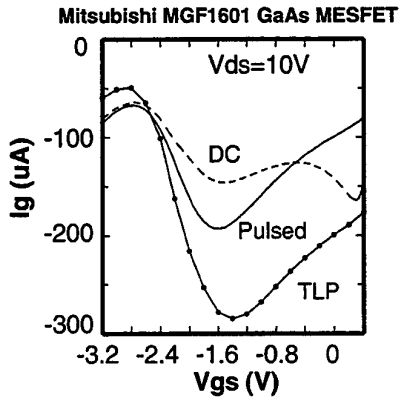


Figure 8: DC, pulsed and 500 ns TLP Ig vs Vgs in the tested GaAs MESFETs at fixed Vds=10V.

We conclude that not only DC, but also 1ms-pulsed measurements with 1% duty cycle are affected by thermal effects, which can lead to an incorrect evaluation of breakdown voltage; therefore only TLP measurements offer the possibility of a correct determination of the Id-BVds breakdown curves.

## 2.4 On-State Breakdown Measurements by Means of Transmission Line Pulses

In the following, we will describe the results of on-state TLP testing of the devices schematically described in Table I. The aim of these measurements was to characterize on-state breakdown effects at very high drain currents and voltages, well beyond the safe operating area of the devices, in order to understand mechanisms which can lead to device burn-out. In this series of measurements, we will assume that on-state breakdown takes place when the device output conductance ($g_D=dI_D/dV_{DS}$) increases catastrophically. This does not correspond to the definition of on-state breakdown adopted in [8], because the $g_D$ abrupt increase usually occurs when the gate current density remarkably exceeds the conventional value of 1mA/mm. However, this definition of on-state breakdown is more adequate for the study of electrical overstress phenomena consisting in large drain voltage or current pulses. It should be stressed that the output conductance can not be reliably measured in DC, because its value is strongly affected by thermal effects. Figure 9 compares the DC and TLP measurements of Id vs Vds characteristics in a Mitsubishi MGF1403 MESFET. The shaded area is the safe operating area of the device, as suggested by the device supplier. The effect of device self-heating on the output conductance of the device is clearly visible in the DC measurements. TLP on-state breakdown measurements are also reported in Figs. 9 and 10. For $V_{DS} > 10$ V, a large increase in $g_D$ takes place; this increase identifies the area where device burn-out is a likely event, see Figure 10.

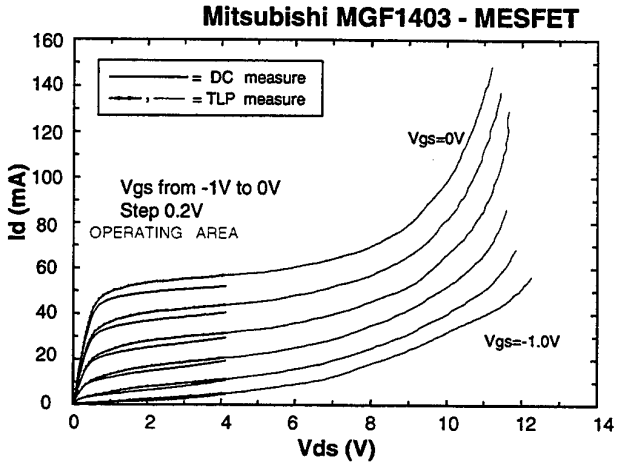


Figure 9: DC (continuous line), and 500 ns TLP (circles and light line) Id vs Vds characteristics

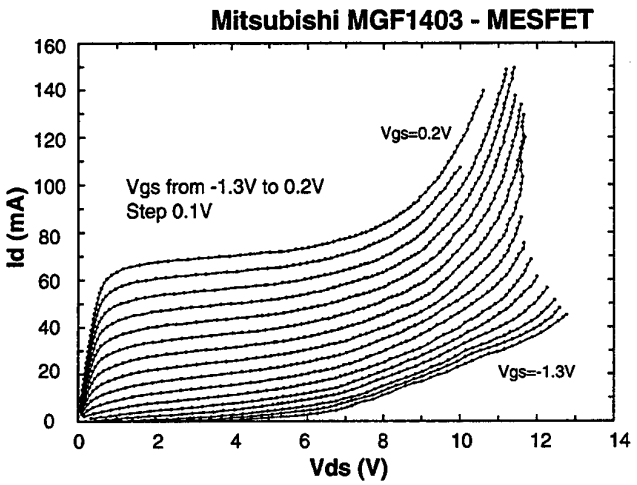


Figure 10: Id vs Vds 500 ns TLP measurements in a Mitsubishi MGF1403.

The same on-state breakdown behaviour is observed in the case of medium power MESFETs Mitsubishi 1601B, see Figures 11 and 12, but in this case we also observe another effect taking place for the most negative gate-source voltages, consisting in a "snap-back" of the I-V curve (i.e. a sudden decrease of the drain voltage on increasing the device current), similar to that observed in the breakdown characteristics of Si MOSFETs [10]. This effect has been already described by Vashchenko and coauthors in [11].

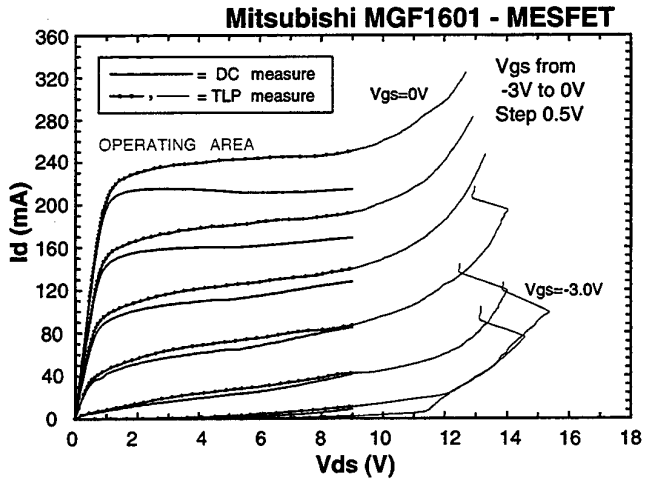


Figure 11: DC (continuous line) and 500 ns TLP (light line and circles) Id vs Vds measurements in tested Mitsubishi MGF1601.

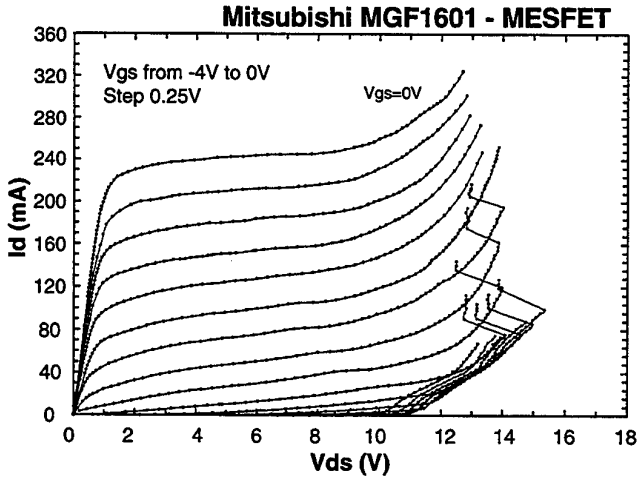


Figure 12: 500 ns Id vs Vds measurements in tested Mitsubishi MGF1601.

Both the described on-state breakdown behaviour and the 'snap-back' in the I-V characteristics are observed also in AlGaAs/GaAs and pseudomorphic HEMTs, see Figs. 13-18 and 19-20, which refer to Toshiba S8902 and Mitsubishi MGF4317D, respectively. For these devices we have been able to reach very high drain current densities ($I_D/W$ = 750 mA/mm and 1 A/mm for S8902 and MGF4317D respectively), where the drain current tends to saturate at a level which depends on the gate source voltage, see Figs. 14 and 20.

In the region where the drain current and output conductance increase, e.g. $V_{DS}$>8 V in Figure 13, also the gate current reaches very high levels. In the Toshiba S8902 HEMT we have been able to measure, *in a non-destructive way,* gate current densities (during 500 ns TLP pulses) up to 30 mA/mm, which is thirty times the value conventionally adopted to define breakdown, see Figure 15 [8].

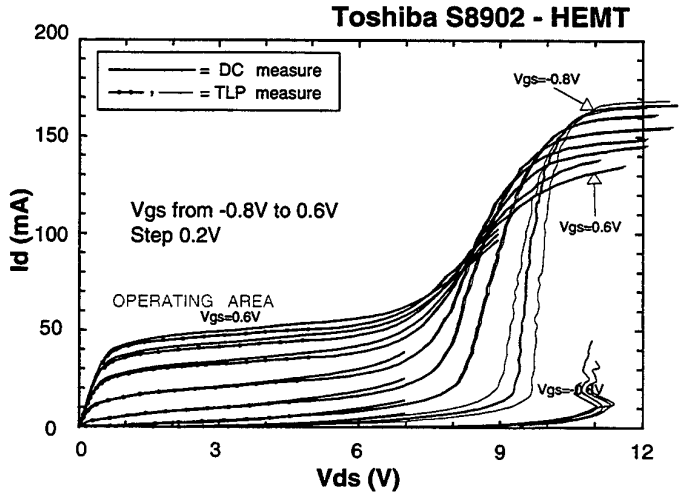


Figure 13: DC (continuous line) and 500 ns TLP (light line and circles) Id vs Vds in tested Toshiba S8902.

The 500 ns TLP measurements of a Toshiba S8902 HEMT are reported in figure 14 . The TLP measurements are obtained by sampling the bias pulses at 500ns.

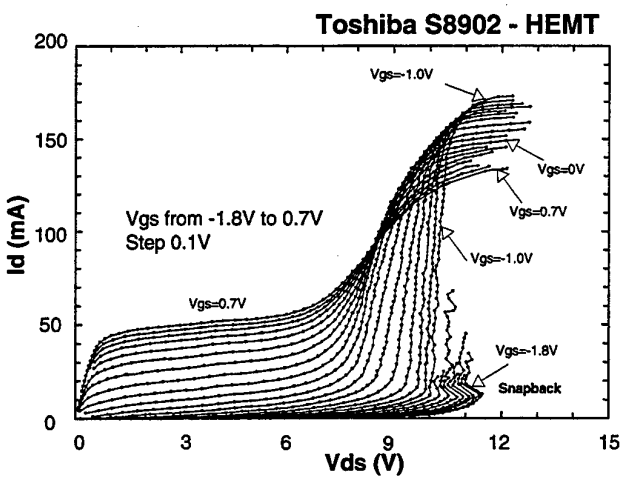


Figure 14: 500 ns TLP Id vs Vds in the tested AlGaAs/GaAs HEMTs (Toshiba S8902).

The drastic reduction in thermal effects allows one to measure the device in extreme conditions without the risk of burn-out (the adopted Vds voltage is three times the absolute maximum rating indicated in the data sheet, Vdsmax=4V).

In breakdown conditions a large increase in Id is observed. The increase in output conductance, typically associated with device degradation and burnout, is very sharp close to device pinch-off, and increases more gradually as the channel is open. Differently from what occurs at relatively lower $V_{DS}$ [12], the gate current level monotonically increases as $V_{GS}$ is decreased, see Fig. 15.

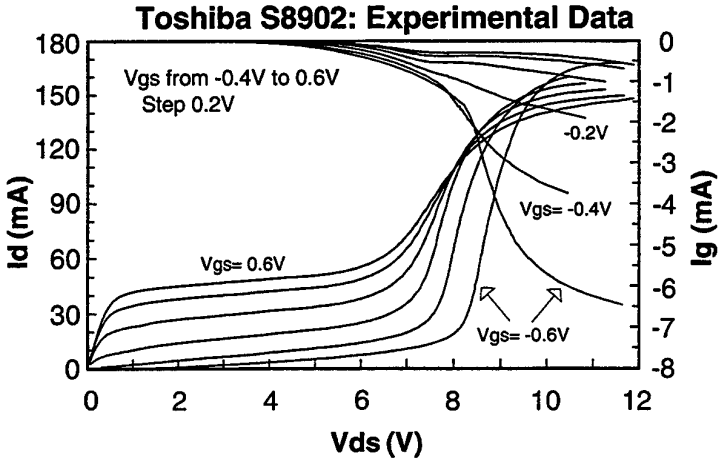


Figure 15: Id and Ig current measured in GaAs HEMT using the TLP set up.

The locus at constant output conductance $g_D$ roughly correspond to those at constant gate current $I_G$, see Figure 16.The output conductance of the devices has the same behaviour of the gate current as a function of $V_{GS}$, see Figure 17.

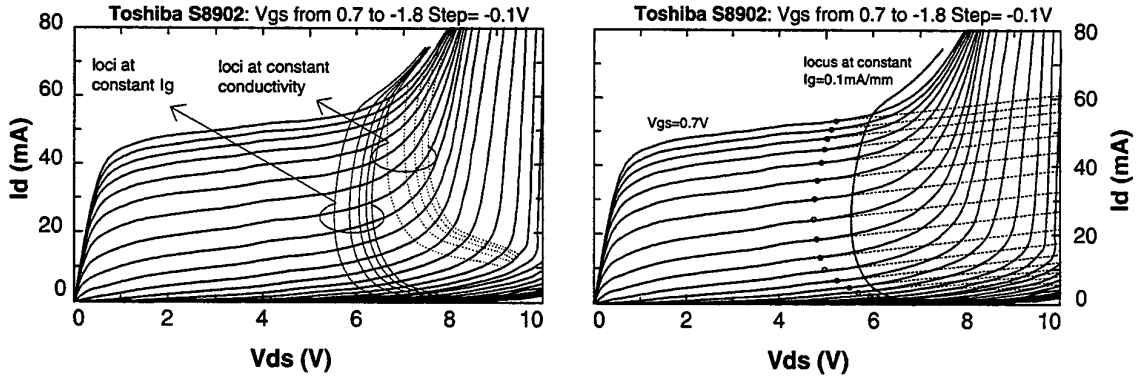


Figure 16: Left: comparison between the loci at constant gate current (from 0.1mA/mm to 0.5mA/mm, tep 0.1 mA/mm) and the loci at constant conductivity (from 150mS to 350mS, step 50mS). The Id vs Vds curves were obtained by sampling TLP pulses at 50ns. Right: comparison between a locus at constant current gate (0.1mA/mm) and the points in which the Id vs Vds curves deviate from linear behavior. The Id vs Vds curves were obtained by sampling TLP pulses at 50ns.

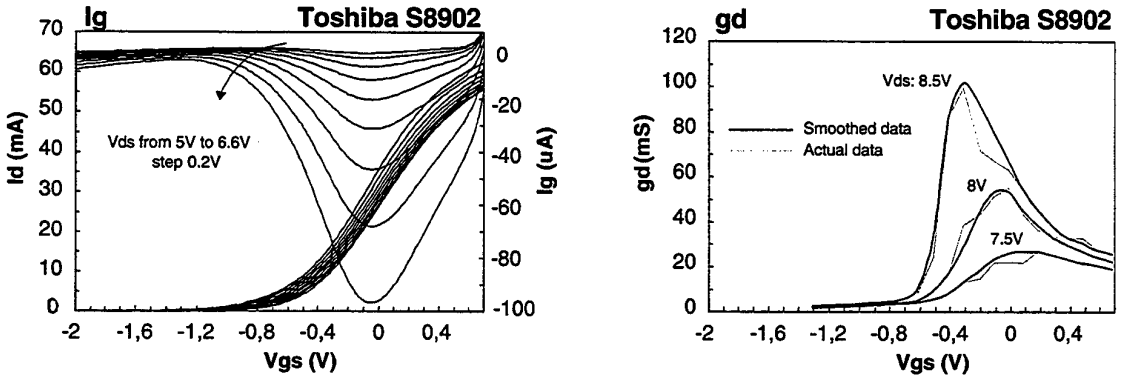


Figure 17: Left: gate current Ig in a Toshiba S8902 AlGaAs/GaAs measured as a function of Vgs with contant Vds (from Vds = 5 V to 6.6 V; DC measurements). Right: Output conductance gD=dID/dVDS in the same device, measured at high VDS (from VDS = 7.5 V to 8.5; 500 ns TLP measurements) in on-state breakdown conditions.

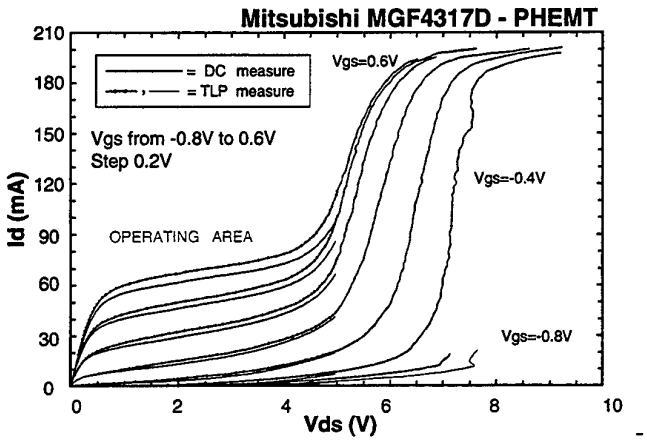


Figure 18: DC (continuous line), and 500 ns TLP (circles and light line) Id vs Vds in tested Mitsubishi MGF4317D.

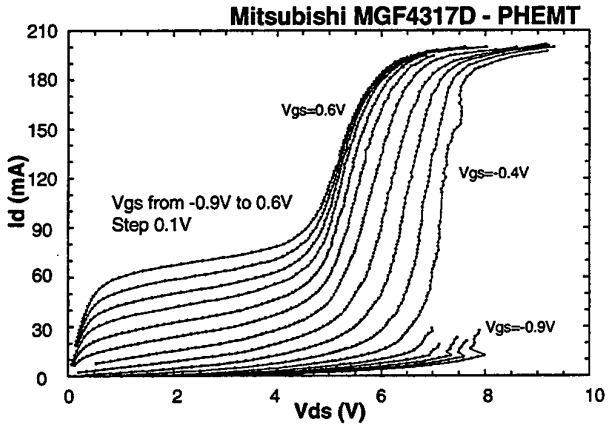


Figure 19: 500 ns-TLP Id vs Vds measurements in a Mitsubishi MGF4317D GaAs MESFET. Snap back phenomena are present for Vgs<-0.6V.

We have also tested some laboratory prototypes of AlGaAs/InGaAs pseudomorphic HEMTS which were affected by the presence of deep levels in the recess region under the gate. A full description of the behavior of the traps in these devices and of their influence on the electrical characteristics has been reported in [3], [13] and will not be repeated here.

The presence of traps enhances kink phenomena in the devices, since trapped electrons lead to drain current reduction at low $V_{DS}$ values. At high $V_{DS}$, the electrons are either de-trapped or compensated, the drain current recovers, thus resulting in a 'kink' in the output characteristics, see Fig. 20. Three effects can contribute to detrap or compensate the trapped electrons: (i) hot electrons can impact ionize traps, thus releasing the trapped negative charge, (ii) the high electric field existing between gate and drain can enhance the electrons detrapping, (iii) holes, generated by impact ionization, can compensate trapped electrons. Since the capture and emission times of the traps are relatively slow, the device transconductance and the kink characteristics depend on the frequency of the signal applied.

Figure 20 shows the comparison between DC, pulsed (1ms/100ms) and 500 ns TLP measurements of the Id(Vds) characteristics of the tested pseudomorphic HEMTs. During pulsed measurements, due to trapping/de-trapping phenomena, steady state values of current and voltages are reached after a transient whose length is determined by the intensity of the gate-drain electric field and, consequently, by the Vgd value. A higher electric field corresponds to a shorter steady state transient time. The amplitude of the kink is therefore lower, and the kink occurs at higher $V_{DS}$ when shorter pulses are adopted, see Fig. 21.

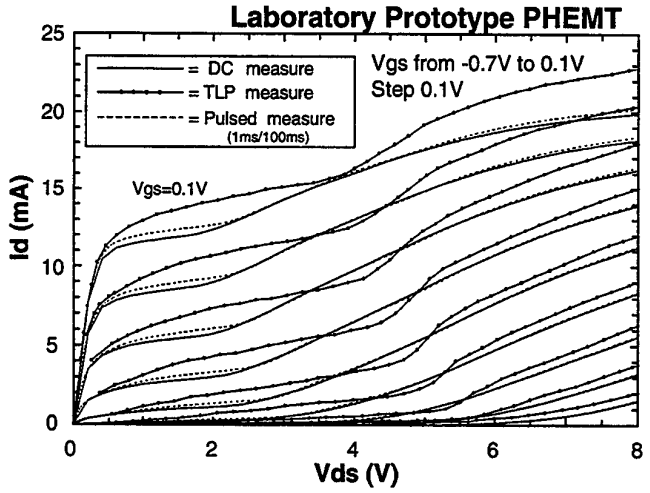


Figure 20: DC (continuous line), pulsed (dashed line) and 500 ns-TLP (circles) Id vs Vds characteristics in a AlGaAs/InGaAs prototype pseudomorphic HEMT.

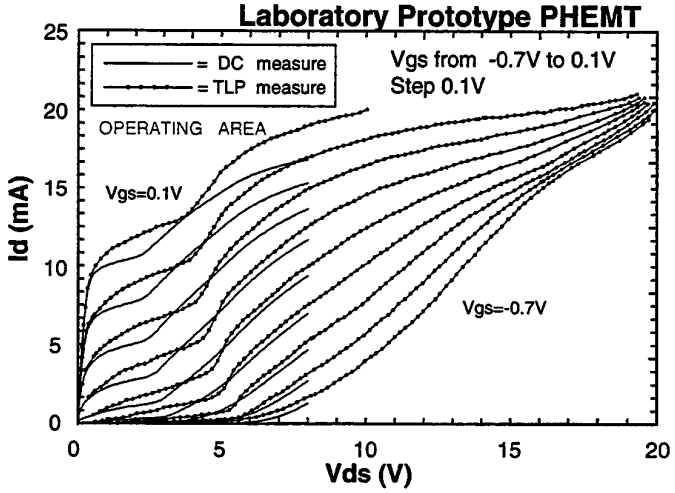


Figure 21: DC (continuous line), and 500 ns-TLP (circles) Id vs Vds in the tested pseudomorphic HEMT.

## 2.5 Summary of TLP Testing Results

Summarizing the results of on-state breakdown measurements at high drain currents and voltages which are common to all tested MESFETs and HEMTs, we can notice the following features:

(a) at increasing $V_{DS}$, all devices show a remarkable increase in the drain current and output conductance. The increase in output conductance follows the non monotonic behaviour of the $BV_{DS}$ ($@I_G/W$=constant) breakdown voltage as a function of $I_D$ or $V_{GS}$. The increase in $g_D$depends non-monotonically on $V_{GS}$, as $I_g$ does, see Figure 17. The locus of constant $g_D$ in on-state breakdown conditions has the same shape as the $BV_{on}@I_{G=constant}$ locus, see Fig. 16.

(b) in the pinch-off region, a regenerative effect may be triggered, which leads to a 'snap-back' of the I-V characteristics, and to a very steep increase in $I_D$, see Figs. 12, 14, and 19. In this region of the characteristics, high electric fields are present, and impact-ionization is very strong, see Fig. 15. This is the most dangerous region, where instantaneous burn-out can easily takes place. In open channel conditions the electric field is lower and the breakdown more gradual.

(c) at very high drain currents, a 'quenching' effect may arise, which limits the increase in drain current and leads to a saturation of $I_D$ as a function of $V_{DS}$, see Figs. 14 and 19.

(d) despite the large increase in Ig/W which takes place during TLP measurements, the drain current does not diverge. Most notably, in open channel conditions, close to maximum drain current levels, avalanche conditions are *never* reached. In general, the abrupt increase in $I_D$ occurs at $V_{GD}$ values higher than the gate-drain breakdown voltage of the gate Schottky diode (measured at source floating, $I_S$=0 mA), reflecting the decrease in the gate-drain electric field which takes place when the device is operated as a transistor with respect to the diode, two terminals configuration.

By driving the devices with the TLP current pulses, the above described regions of device operation can be studied without any catastrophic degradation effect such as burn-out. Only some of the devices have suffered slight changes of their electrical parameters ($V_T$, $g_m$) due to hot-carrier degradation [14].

## 2.6 Monte Carlo Simulation and Compact Spice Modeling of MESFET's and HEMT's Breakdown

Several authors [15]-[19] have described a parasitic bipolar effect in MESFETs and HEMTs, due to the holes generated by impact ionization, and capable of causing a positive feedback mechanism which can lead to device breakdown. This explanation has been adopted to justify weak-medium avalanche conditions or kink phenomena; its validity when remarkable impact-ionization effects are present has not been demonstrated.

In the following, we will use a 2D Monte Carlo device simulator and a simple SPICE-like circuit model with the aim of explaining the experimental features of on-state breakdown at high drain current and voltages, which have been described in the previous Section.

### 2.6.1 Monte Carlo simulations

A better understanding of on-state and off-state breakdown mechanisms of HEMTs has been achieved in recent years [15]-[20]; in particular, experimental and theoretical analysis have shown that one mechanism leading to on-state breakdown is the accumulation, in the channel and in the buffer or donor layers between gate and source, of holes generated by impact- ionization [15]-[20]. Accumulation of holes enhances injection of electrons, which induces further impact-ionization.

This mechanism may lead to device breakdown and burn-out, and causes an increase in output conductance and "kink" effects. Most of the above mentioned studies, however, refer to DC conditions, and only a few analysis have considered high frequency pulsed behavior, which could be more relevant for microwave and millimeter-wave applications of HEMTs. Vashchenko et al. [11] have studied drain breakdown of GaAs MESFETs in the ns and sub-ns range and demonstrated that a portion of holes that were generated near the drain is accumulated in the SI buffer near the $n^+$ source contact, and that device burnout can take place in sub-ns times. J.P.R. David et al. [21] estimated the time until breakdown as a function of gate-drain voltage in excess of BVgd in GaAs MESFETs; they calculated typical times in the 20 - 240 ps range. More recently, G. M. Dunn et al. [22] carried out a Monte Carlo simulation of impact ionization in 1.2 μm MESFETs and show that accumulation of holes and electrons can also be correlated with the onset of oscillations with a typical period of 5-10 ps. In the following we will describe the dynamical behavior of breakdown effects in 0.25 μm double heterojunction HEMTs by means of a Monte Carlo simulation.

A 2D self-consistent Monte Carlo code, accounting for 3 conduction valleys and 3 valence bands has been adopted. Poisson equation is solved by applying a multi-grid technique [23]. Impact ionization has been described by a modified Kane model [24], with parameters chosen so as to reproduce the experimental ionization coefficients of strained InGaAs measured by David and coworkers [25].

The general-purpose weighted Monte Carlo procedure (100000 electrons) presented in [24] has been adopted to achieve a correct description of the physics of HEMT breakdown. We simulated a 0.25 μm double heterojunction AlGaAs/InGaAs HEMTs, whose schematic cross section is depicted in Fig. 22. Experimental characteristics have been described in [26]. An $n^+$ region was introduced under the source and drain metallic contacts (see grid area in Fig. 24) in order to facilitate electron injection into the channel and to properly reproduce the ohmic portion of the measured I-V characteristics.

When the HEMT is biased at high drain voltage ($V_{DS}$ > 4 V), the strong electric field at the gate-end of the channel heats up the electrons to energies where they start impact ionizing. Correspondingly, the drain current increases abruptly (solid curve in Fig.23). A comparison with the dashed curve in Fig.23, obtained from a simulation where impact ionization is inhibited, demonstrates that such behaviour is directly related to ionization processes. As a result of each impact ionization process, an electron-hole pair is created. The electron is pushed towards the drain, contributing to the outgoing current. The hole is either attracted by the gate potential, or moves backward towards the source.

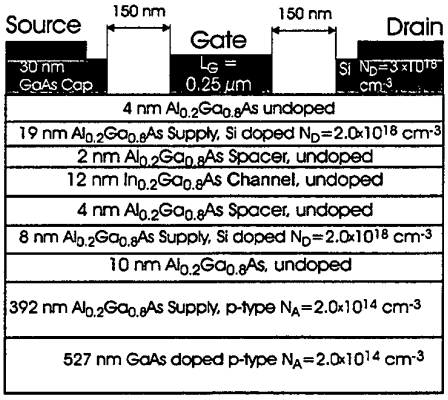


Figure 22: Schematic cross section of the simulated double heterojunction HEMT

The actual hole distribution in the active portion of the device is shown in Fig. 24 for two different times after impact ionization has been switched on. The simulation has been performed as follows: a steady state condition is first reached without impact ionization (as for the dashed curve of Fig. 23). Then, the impact ionization is turned on (t = 0) and both electrons and holes are followed in their dynamics.

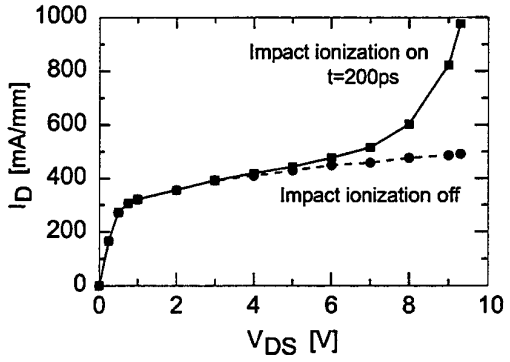


Figure 23: Simulated output characteristics for VGS = -0.2 V with and without impact-ionization

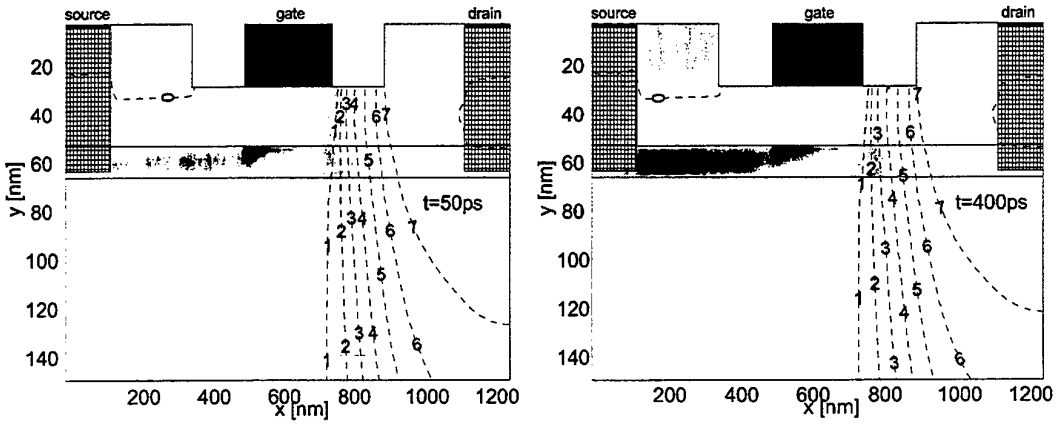


Figure 24: Hole density at two time values (50 ps, left; 400 ps, right) after switching-on of the impact ionization (VDS = 8 V, VGS = -0,2 V, T = 300 K)

Figure 24 also shows the contourn lines of the internal potential. The holes are generated by the channel electrons in the high field region at the gate-end of the channel. Some of them (just a few percent) overcome the barrier at the InGaAs/AlGaAs heterointerface and are then collected by the gate contact, contributing a current of a few mA/mm. Around thirty five percent of the generated holes remain confined in the channel and move towards the source contact, while the remaining ones diffuse into the substrate. As time evolves (Fig. 24, right), a considerable hole concentration builds up at the source-end of the channel and in the substrate, creating a positive space charge region. It has been previously suggested that the accumulation of positive charge near the source contact leads to an increase in output conductance in GaAs MESFET [18], [19], SOI MOSFETs [27], InAlAs/InGaAs HEMTs [28], and in InAs/AlSb HFETs [29],[30].

This so-called *parasitic bipolar effect* (PBE) is due to the fact that holes escaping into the substrate of such devices act as a parasitic back gate, which in turn leads to an increase in the electron current flow in the channel. Consistent with the analysis of the hole dynamics made above, we expect that a PBE is responsible for the current increase shown in Fig. 23. As a first check, we have verified that ionization events initiated by secondary carriers are negligible.

In order to evaluate the contribution of the impact ionization current (that is the direct effect of the enhancement in the number of carriers when ionization occurs), we have performed a series of computer experiments whose results are presented in Fig. 25. The curves labelled *impact ionization off* and *$e^-/h^+$ pair generation* refer respectively to simulations where impact ionization is always off or is turned on at t = 0. The steady state current values correspond to those of Fig. 23 (dashed and solid lines, respectively) for a drain bias of 8 V. The separate electron contribution can be evaluated by artificially allowing only secondary electrons (and not holes) to be created at each ionization process. The current response (curve labelled *$e^-$ generation only* indicates a minor contribution of the secondary electrons to the drain current. On the contrary, if only secondary holes (and no secondary electrons) are created, the current enhancement is considerable. Steady state is reached in this case in a few hundreds of picoseconds, an evidence that hole transport processes do control the dynamical behavior of the device.

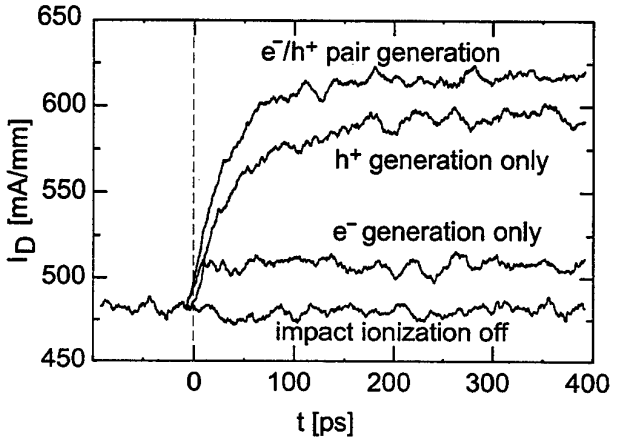


Figure 25: Time dependence of Id for several types of simulation, considering or omitting secondary carriers. At t=0 the impact ionization processes are switched-on (VDS = 8 V, VGS = -0,2 V, T = 300 K

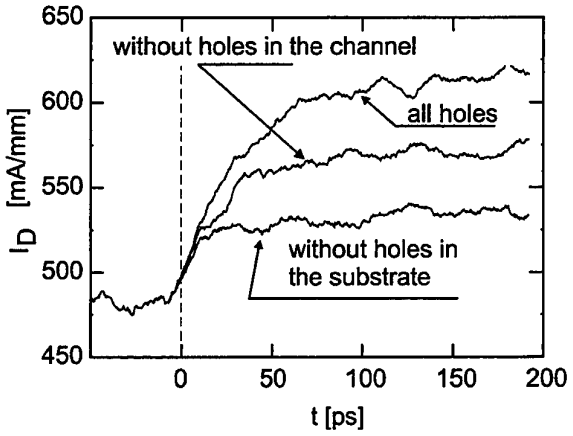


Figure 26: Simulated time dependence of drain current showing the different contribution due to the hole in the channel and in the substrate. At t=0 the impact ionization processes are switched-on (VDS = 8 V, VGS = -0,2 V, T = 300 K)

A further simulated experiment illustrates the origin of the PBE in our HEMT (see Fig. 26). By selectively removing holes from different regions of the device before solving Poisson equation, it is possible to isolate the space charge contribution from such regions. If, for instance, the substrate holes are not considered, the current reaches a steady value much lower than that obtained both in the "standard" simulation (i.e. when all holes are considered), and if the channel holes are neglected. Such results confirm that the increased drain current of this device, biased close to breakdown, originates mainly from the accumulation of holes in the substrate region, and to a minor extent in the channel, which, in turn, gives rise to an enhanced drain current via a parasitic bipolar effect. By inserting a p-type contact that collects the accumulated holes, the parasitic effect almost completely disappears and the simulated on-state breakdown voltage shifts to higher values. A similar finding had been previously presented in relation to the kink characteristics of HEMTs [31], [32].

Concluding this Section, a detailed Monte Carlo analysis of impact-ionization in AlGaAs/InGaAs pseudomorphic HEMTs has been presented. The simulation shows that accumulation of holes generated by impact-ionization takes place in the channel and substrate regions near the source contact. The presence of the positive space charge favours the injection of electrons from the source, thus leading to significant increase in drain current. Such complicated feedback, which triggers on-state breakdown in HEMTs, has characteristic times in excess of 100 ps. Thus, the effects of impact-ionization under rf or pulsed drive may be significantly different from those observed in DC.

## 2.7 Circuit-Level Modeling of Impact Ionization in MESFETs and HEMTs

Experimental data and Monte Carlo simulations show, in agreement with the literature [15]-[20], that the holes generated by impact ionization induce a parasitic bipolar effect (PBE) leading to the described anomalies. They also allow one to derive the information needed to develop a simple circuit-level model of the effects of impact-ionization on MESFETs and HEMTs, suitable for SPICE-like circuit simulation, which is described in the following.

The aim of this part of the work was to obtain a model capable of describing device characteristics up to breakdown, thus representing correctly both the gate current and the increase in drain current and output conductance.

The developed SPICE model, Figure 27, is based on the 'Level 4' description of the intrinsic GaAsFET included in the PSPICE™ circuit simulation program by MicroSim™ [33]-[39]. This basic model has been completed by adding other elements which describe impact-ionization and related parasitic phenomena, i.e.:

(a) a gate current generator ($I_{gate}$ in our circuit) which describes the increase in gate current due to holes generated by impact-ionization and collected by the gate;

(b) a source voltage generator $\Delta V_s$, which describes the modulation of channel current due to the holes accumulated in the channel or substrate source region. This effect is responsible of the 'kink' phenomena occurring at weak ionization level [40]. It should be stressed that, due to the finite value of the FET transconductance, this effect alone can not explain the very large increase in drain current which have been observed by TLP measurements. It can, on the other hand, explain a kink of amplitude $\Delta I_D = g_m \Delta V_{GS}$, which can be enhanced by the presence of traps [15].

(c) a parasitic NPN bipolar transistor with emitter and collector connected to source and drain respectively, having the base driven by the hole current generated by impact-ionization ($I_b$).

Following the model by K. Hui et al. [7], the following bias dependence was chosen for the two current generators Igate and Ib: $Igate = A_1 I_D \exp(-B/(V_{DG}+V_P))$, $Ib = (A_2 I_D + A_3 I_C)\exp(-B/(V_{DG}+V_P))$, where $V_{DG}$ is the voltage between drain and gate, $V_P$ is the device pinch-off voltage, $I_C$ is the collector current of the parasitic bipolar, $I_D$ is the drain current of the intrinsic FET, and $A_1$, $A_2$, , $A_3$ and B are fitting constants.

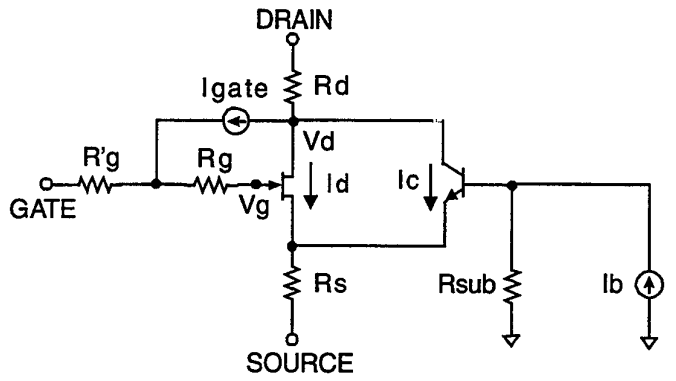


Figure 27: SPICE-like circuit adopted to simulate breakdown characteristics.

The model not only predicts correctly gate current and on-state breakdown at fixed $I_G/W$, see Figs. 28 and 29, but also describes the abrupt increase in $I_D$ induced by the parasitic bipolar effect, and the snap-back, see Figures 30 and 31.

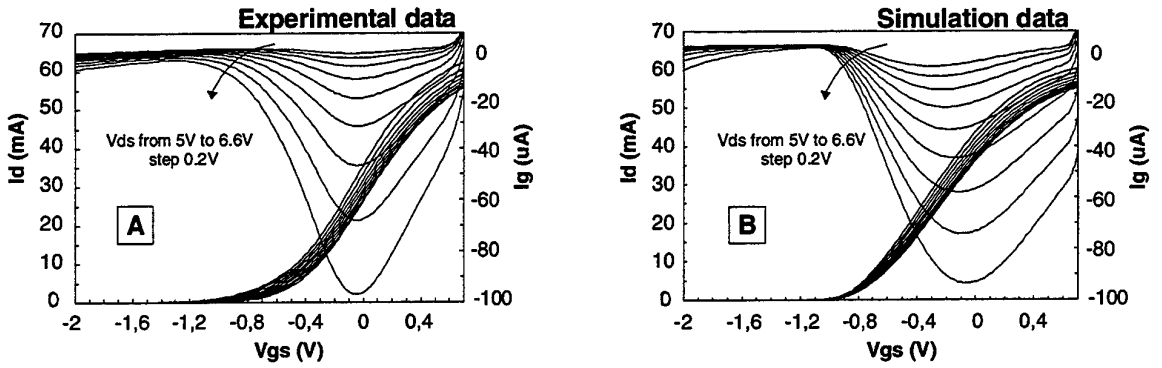


Figure 28: Measurements (A) and simulations (B) of the gate and drain currents vs Vgs in weak ionization conditions, in a Toshiba S8901 AlGaAs/GaAs HEMT.

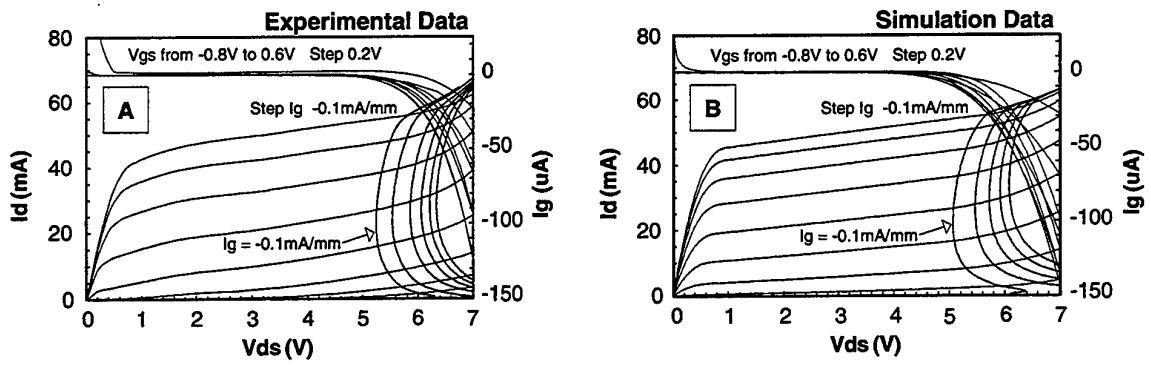


Figure 29: Measurements (A) and simulation (B) of the gate and drain current vs. VDS in the tested AlGaAs/GaAs S8901 Toshiba HEMTs. The ID vs BVon on-state breakdown loci measured at various values of gate current densities are also reported.

If simulated and experimental output characteristics in on-state breakdown conditions are compared, Figure 30, it becomes evident that the effect of saturation in the drain current at very high drain voltages and current densities is not taken into account by the model. In fact, the model as it is neglects thermal effects and high-injection phenomena occuring in the parasitic bipolar transistors; both these effects contribute to limit the $I_D$ increase, as it will be explained in the following.

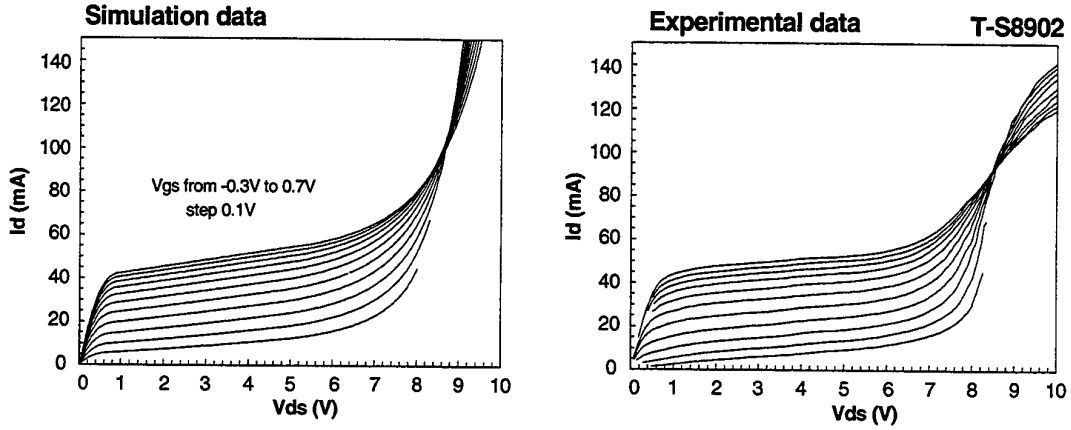


Figure 30: Left: PSPICE™ simulations of on-state breakdown characteristics in a Toshiba S8902 HEMT. Right: experimental on-state breakdown characteristics measured in a Toshiba S8902 HEMT by means of 500 ns TLP pulses.

The derived model predicts correctly the occurrence of snap-back in pinch-off conditions, see Fig. 31.

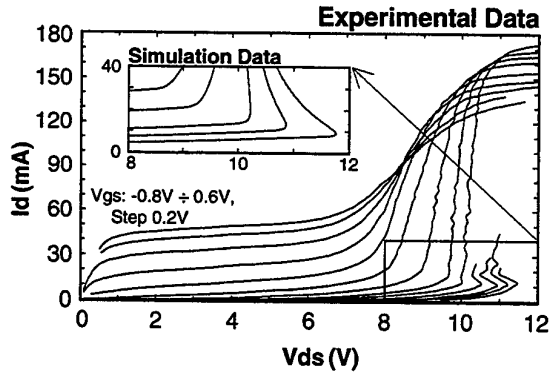


Figure 31: 500 ns TLP ID(VDS) characteristics of a Toshiba S8902 HEMT. Inset: PSPICE™ simulation of snap-back effects.

# 2.8 Study of the Dynamic Behaviour of Drain Current

Figure 32 depicts the typical behaviour of the drain voltage and current pulses during TLP testing of a representative device (Toshiba S8902 HEMT). When device power dissipation is significant, i.e. at very high $I_d$ and $V_{ds}$ values, the measured value of $I_D$ decreases during the pulse, while $V_{DS}$ increases since the set-up is trying to keep the device current constant. In order to rule out possible parasitics of the meaurement set-up, we carried out the same measurements, at the same current level, on calibrated non-inductive resistors, obtaining nearly perfect current and voltage pulses.

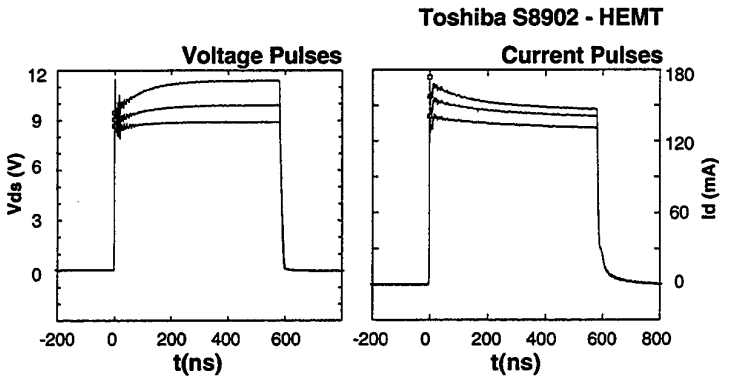


Figure 32: TLP voltage and current pulses measured at Vgs=0.6V in the Toshiba S8902 HEMT, at increasing the charging voltage of the line, Vdd in Fig. 1.

The phenomenon is therefore intrinsic to the tested devices. If we sample the drain currents and voltages at different times during the TLP pulse and we plot the corresponding I-V curves, we obtain the results shown in Fig. 33. Notice that if we extrapolate the current level at a sampling time t= 0 ns, the drain current increases linearly with $V_{DS}$, with a high output conductance, as it occurs in the SPICE simulations. Figure 34 shows the difference between the 50 ns and the 550 ns I-V characteristics for various gate voltages. Notice that, the characteristics at lower gate voltages (higher gate-drain electric fields) tend to reach higher levels of drain current, despite the presence of the saturation effects.

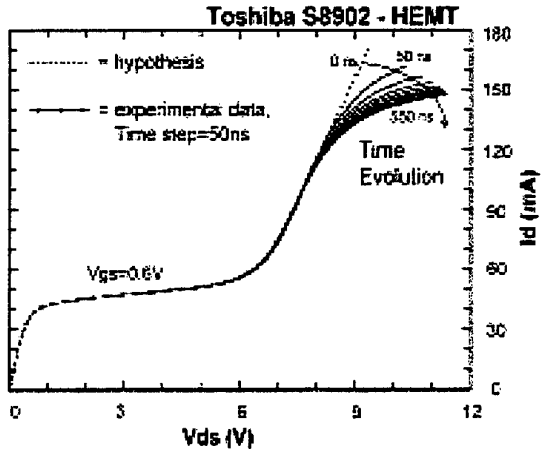


Figure 33: TLP ID(VDS) measurements at VGS=0.6 V, obtained by sampling the current and voltage values at various times during the pulse. The device under test is a Toshiba S8902 HEMT.

An even more pronounced drain current saturation effect is observed during DC or 1 ms-pulsed measurements of on-state breakdown, see Figure 35.

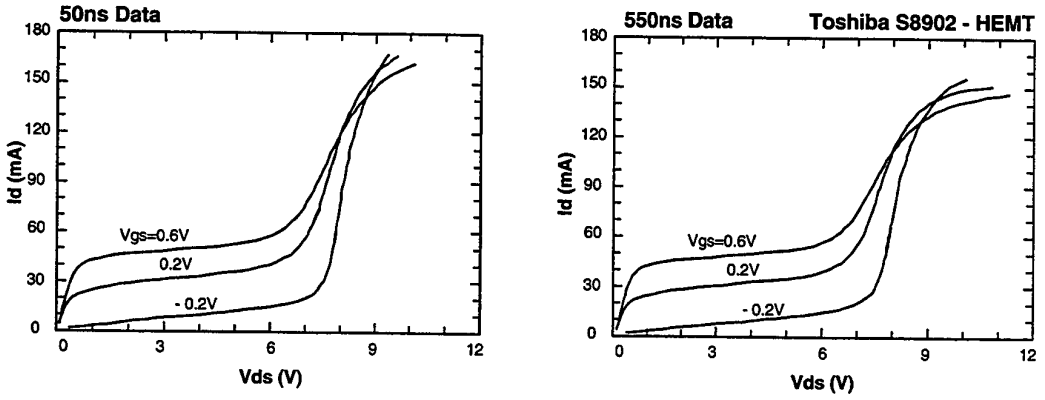


Figure 34: TLP measurements of Id vs Vds curves obtained sampling the voltage and current after a delay time of 50ns and 550ns. Tested device: Toshiba S8902 HEMT.

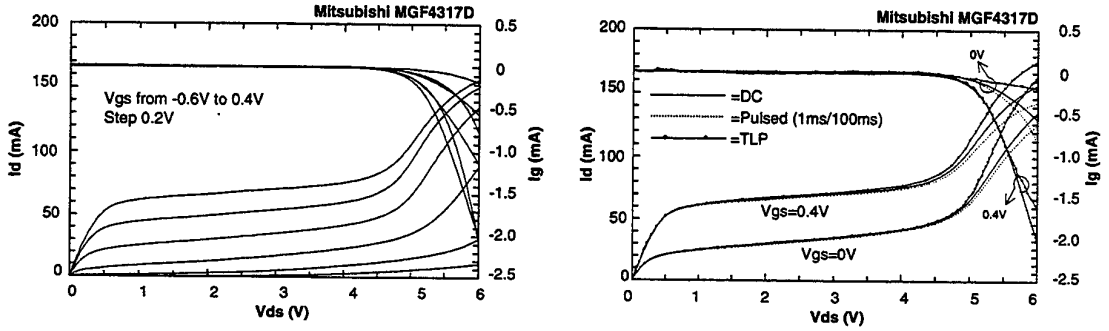


Figure 35: (a) DC measurements on Mitsubishi MGF4317D, GaAs MESFET; (b) comparison between DC, pulsed (1ms/100ms) and 500 ns TLP measurements for Vgs=0 and 0.4V.

The various I-V curves depicted in Fig. 35 have been obtained with the same number of measurement points, in order to keep the average power dissipation of the device fixed. At increasing the pulse duration, the drain current tends to decrease at increasing $V_{DS}$, see Figure 36, and destructive breakdown is not reached even at voltages in excess of 12 V, with gate currents larger than 5 mA !

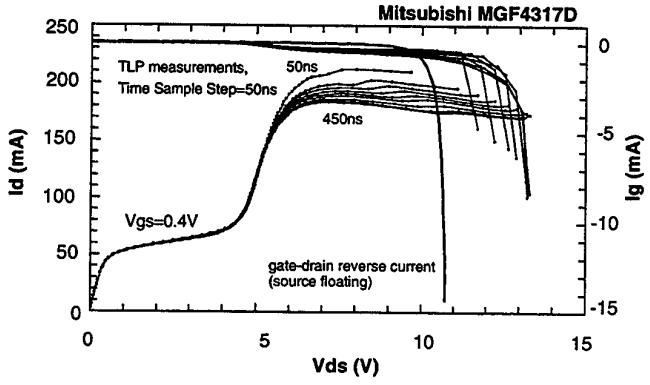


Figure 36: TLP measurements of Id, Ig vs Vds curves, obtained by sampling current and voltage values at different times during the pulse. Tested device: Mitsubishi MGF4317D GaAs MESFET. The thick line represents the gate-drain reverse current measured with source floating (shifted to the left by 0.4 V for consistence with the other curves at VGS0.4 V).

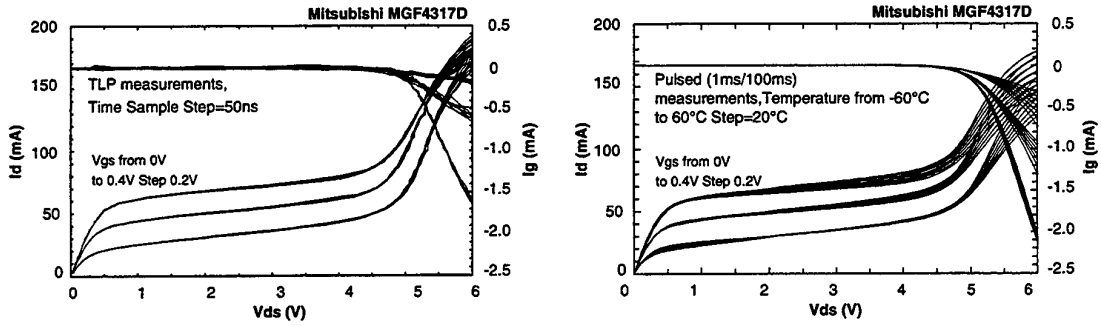


Figure 37: Left: TLP measurements of Id, Ig vs Vds curves, obtained by sampling the TLP pulses at various times. Right: 1 ms pulsed measurements of Id, Ig vs Vds at different ambient temperatures.

The influence of temperature on the on-state breakdown characteristics was studied by means of 1ms-pulsed voltage tests. As shown in Fig. 37, an increase in the device temperature enhances the bending of the I-V curve, and leads to a reduced drain current level after saturation. We therefore ascribe the 'saturation' effect to thermal effects taking place with a relatively fast time constant during the TLP pulses, see Figs. 32 and 33. Since during on-state breakdown at these current levels the device current is mostly due to the parasitic bipolar, high-injection effects reducing the gain of the bipolar transistor and the gate-drain electric field can also induce a reduction in the observed current. The influence of high-injection effects can not be completely ruled out; in fact, I-V curves at lower $V_{GS}$, with higher gate-drain electric field values, reach higher drain current levels and higher device power dissipation levels, see Figure 34.

# 2.9 Conclusions

A new method for the dynamic testing of breakdown and burn-out effects of microwave devices in the 50 ns - 500 ns range has been developed. A wide set of commercially-available devices and laboratory prototypes has been tested, including low- and medium- power GaAs MESFETs, AlGaAs/GaAs and AlGaAs/InGaAs HEMT's on GaAs and InAlAs/InGaAs HEMT's on InP.

The following conclusions can be drawn:

(a) the present methods of on-state breakdown testing, based on DC measurements, are inadequate for the evaluation of power devices, since thermal effects remarkably influence breakdown characteristics.

(b) a simple Transmission Line Pulse set-up can be used for dynamic testing of on-state breakdown with short current pulses, thus reducing thermal effects and enabling on-state breakdown measurements to be carried out up to extremely high levels of gate current density. This set-up allows one to perform a more realistic evaluation of the device resistance to electrical overstress, and of its survivability. This new pulsed testing system will be particularly useful for the testing of power devices based on wide band-gap semiconductors.

(c) experimental results and Monte Carlo simulations show that on-state breakdown in III-V FET devices is not simply due to carrier multiplication caused by impact-ionization and avalanche, but is the results of a parasitic bipolar action (PBA), induced by the generated holes, which enhances the electron current. Due to the PBA, the electron current injected into the device high field region increases, and this at its turn increases hole generation by impact-ionization. The two effects, combined, give rise to a positive feedback mechanism which is particularly dangerous closed to pinch-off conditions, where it can induce 'snap-back' of the output characteristics, or catastrophic device burn-out.

(d) in open channel conditions, at high $V_{GS}$ values, breakdown takes place more gracefully, due to the reduced gate-drain electric field which alleviates the positive feedback action.

(e) An equivalent circuit model which describes impact-ionization and gate current by means of the K. Hui law, and includes a parasitic bipolar transistor in order to model the PBA describes correctly device on-state breakdown characteristics, with the exception of the quasi saturation of drain current due to thermal effects.

(f) Since the PBA is essential to turn on breakdown in on-state, a device structure allowing a fast removal of the generated holes, thus preventing the PBA to take place should show improved breakdown characteristics. For instance, devices adopting a p-type buffer have been shown to be less affected by weak ionization phenomena [ref].

(g) Finally, Monte Carlo simulations have shown that the complicated feedback originated by the PBA, which triggers on-state breakdown in HEMTs, has characteristic times in excess of 100 ps. Thus, the effects of impact-ionization under rf or pulsed drive may be significantly different from those observed in DC.

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